DEVELOPMENT OF CONVECTIVE SOLDER REFLOW AND PROJECTION MOIRÉ SYSTEM AND FEA MODEL FOR PWBA WARPAGE PREDICTION

A Dissertation
Presented to
The Academic Faculty

By

Reinhard Edison Powell

In Partial Fulfillment
Of the Requirements for the Degree
Doctor of Philosophy in the
George W. Woodruff School of Mechanical Engineering

Georgia Institute of Technology
May 2006

DEVELOPMENT OF CONVECTIVE SOLDER REFLOW AND PROJECTION MOIRÉ SYSTEM AND FEA MODEL FOR PWBA WARPAGE PREDICTION

Approved by:

Dr. I. Charles Ume, Advisor
School of Mechanical Engineering
Georgia Institute of Technology

Dr. S. Mostafa Ghiaasiaan
School of Mechanical Engineering
Georgia Institute of Technology

Dr. Jiahui Pan
Akrometrix, LLC

Dr. Russell S. Peak
Manufacturing Research Center
Georgia Institute of Technology

Dr. Suresh Sitaraman
School of Mechanical Engineering
Georgia Institute of Technology

Dr. C. P. Wong
School of Materials Science and Engineering
Georgia Institute of Technology

Date Approved: April 7, 2006

To my mother Pamella, for her sacrifices, undying support and encouragement throughout all my life endeavors. I am not sure why I am deserving of such a great mother. I will be eternally grateful.

ACKNOWLEDGEMENTS

The completion of PhD degree requires the cooperation of many beings. First, I would like to thank God for allowing me to be alive and healthy, and for guiding me through my life endeavors.

I would like to thank my advisor, Professor Charles Ume for this support during my six years in graduate school. Dr. Ume supported me even when my progress was slow and often provided me with life advice in addition to academic advice as well as lots of free meals over the years. His guidance has been greatly appreciated.

I would like to thank the other members of my PhD Thesis Reading Committee: Dr. S. Mostafa Ghiaasiaan, Dr. Jiahui Pan, Dr. Russell Peak, Dr. Suresh Sitaraman and Dr. C. P. Wong for agreeing to serve on my committee and for providing useful suggestions during my proposal presentation.

I would also like to thank the Manufacturing Research Center Manufacturing Education Program as well as the Sam Nunn Security Program for funding.

I would like to thank Mr. Alex Goldstein and Dr. Yeong Kim for allowing me access to the CBAR and PRC facilities for my test vehicle assembly.

I would also like to acknowledge my colleagues in Dr. Ume's group, Dr. Hai Ding, Dr. Akio Kita, Lizheng Zhang, Wei Tan, Carl Hanna, Matt Rogge and Jin Yang for their useful suggestions and making my graduate school experience more enjoyable.

I would like to thank Professor Sitaraman's students, Andy Perkins and Krishna Tunga for helping me with modeling and teaching me how to use the PRC rework station to place PBGA packages. I would also like to thank my other academic friends, Dr. Ryan

Johnson, Dr. Scott Bondi Dr. Jennifer Muncy, and Mike Colella for fun times and many insightful discussions.

I would like to thank my mother Pamella Powell, my sister Roxanne Powell, and my mother-in-law Pauline Jones for their love and support during my study at Georgia Tech.

I would like to thank my friends Hans Ashman, Don-Marc Hall, Stuart Williams, Andre Pagon, Simon Packer, Ricki Walsh, Joseph Ogilvie and Leanne Minott who have shown me time and time again how important it is to have good friends. I am very grateful to have them in my life.

Finally, but by no means the least, I would like to thank my beautiful and loving wife Tam'ra for her support throughout my PhD program. She has been very patient and supportive and always had encouraging words for me when times were rough. Tam'ra is truly an inspiration to me, and the most amazing person I have ever met. I can only hope that I'm able to do as much for her as she has done for me.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

SUMMARY

Warpage has long been known to cause thermomechanical reliability problems in electronic packaging. Warpage is a global effect of interfacial stress and displacement. The warpage problem in electronic packaging can be further aggravated by thermal processing such as reflow and temperature cycling. In a printed wiring board assembly (PWBA), warpage of the PWB or assembly chip packages may result in chip package misregistration, solder joint failure, die cracking and delamination of the solder bumps between chip packages and the PWB.

In this research, a projection moiré warpage measurement technique capable of measuring PWB/PWBA/chip package warpage during convective reflow processes is developed. The developed system is then used to study the warpage of PWBs populated with plastic ball grid array (PBGA) chip packages along with a finite element (FE) model. To simulate convective reflow, a convective heating subsystem was developed and added to the warpage measurement system. The developed convective system can simulate reflow profiles with heating rates of 0.6 ^{o}C/second and below such as the Lee optimized profile. When compared to the previously used infrared heating system, the developed convective system enables more uniform heating of PWBs/PWBAs. However, the heating rate of the developed convective heating system needs improvement to simulate reflow profiles with heating rates larger than 0.6 ^{o}C/second. To determine methods to improve the convective heating system, a computational fluid dynamics (CFD) model of the system was developed. The CFD model was used to determine convective heating system parameter settings to improve the system's heating rate.

To accurately calculate the warpage of PWBs and chip packages simultaneously, an automated chip package detection algorithm was developed in this research. The algorithm is based on active contours (snakes) and is capable of segmenting up to two chip packages on a PWB. After segmenting the chip package(s), the unsegmented PWB locations are used to calculate maximum PWB warpage which is the difference between maximum and minimum PWB out-of-plane displacements. The segmented chip package location(s) can then be used to calculate chip package warpage.

These new capabilities were used to measure the warpage of a PWB test vehicle with up to two PBGA packages during a convective heating process. The results showed that PWB warpage change during a convective heating process for this particular PWB decreased with the number of PBGA packages assembled on to the PWB. More studies are needed to see if this is the case for other types of PWBAs. Also, for this particular PWB, if the PBGA package is assembled near a PWB corner, that corner tends to have a lower out-of-plane displacement after a convective heating process when compared to other PWB corners.

To supplement the projection moiré warpage experiments, a FE technique was developed to study PWBA configurations not allowed by the available test vehicle. The FE technique was used to study the effect of PBGA package location on PWB warpage. The FE technique was validated using projection moiré experiments, and the results showed that to minimize warpage for this particular PWBA, the PBGA package(s) should be placed close to the PWB edges far away from the center of the PWB.

This dissertation represents a significant contribution to the area of warpage measurement. The first known large area convective heating warpage measurement

system is developed in this research along with the projection moiré technique which can measure PWBs populated with chip packages. The projection moiré results presented in this thesis is the first known work that experimentally studies the warpage of populated PWBs by automatically detecting chip packages and factoring out their height effects.

CHAPTER 1

INTRODUCTION

Over the past 50 years, the electronics manufacturing industry has undergone revolutionary changes, which have provided consumers with a plethora of electronic products. Approximately 50 years ago, silicon based transistors were developed to replace the much more bulky vacuum tubes used in electronics. In the early 1960s, integrated circuit (IC) technology was developed to achieve high functionality and performance while integrating hundreds of transistors on a single chip. Progress in the design of ICs went hand in hand with progress of manufacturing techniques. IC cost was reduced due to continuous miniaturization and lower manufacturing costs as ICs increased in functionality. The number of components, diodes, transistors, and capacitors per chip has increased a hundred thousand times between 1965 and 1995, and hundreds of millions of components can now fit on a single chip. Due to functional and performance requirements of modern and future electronics, the semiconductor industry will experience billions and even trillions of transistors integrated on to a single semiconductor chip [1]. Reliability of electronic components and electronic assemblies has become more of a concern as electronics manufacturing technology becomes more advanced.

Electronic packaging is defined as the bridge that interconnects integrated circuits and other components into a system-level board to form electronic products [2]. Figure 1.1 shows the electronic packaging hierarchy [2]. At the first level of packaging, the electronic packaging serves to interconnect, power, cool and protect ICs. After the first

packaging level, the IC is ready to be assembled on to a printed wiring board (PWB) to form a PWB assembly (PWBA). A PWB falls in level two of the electronic packaging hierarchy, and serves to interconnect every IC component with conductive circuit traces

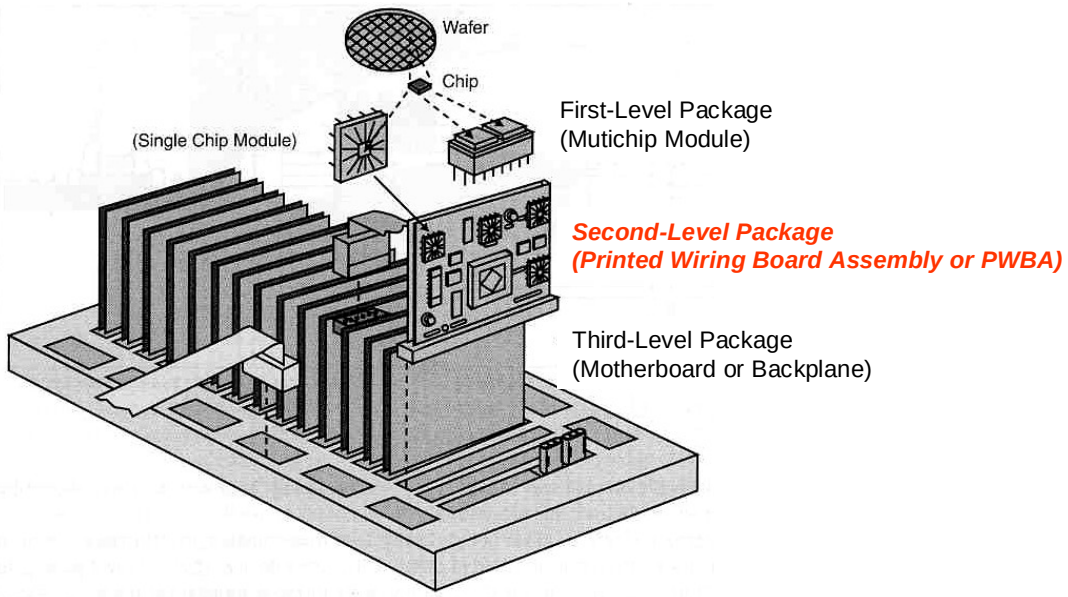


Figure 1.1. Electronic packaging hierarchy [2]

to form one interconnected system. An example of a level two package is a computer memory board which consists of several IC chip packages assembled onto a PWB. Systems that require several PWBAs to communicate with one another will have level three packaging. An example of a level three package is a motherboard or a backplane as shown in Figure 1.1. Assembling a system with all packaging hierarchy levels as shown in Figure 1.1 is a very complicated process and input from many scientific disciplines are necessary in order to streamline the process. This research will focus on the second level of the packaging hierarchy and will revolve around assessing the reliability of PWBAs.

After an electronic product is manufactured, several failure mechanisms can occur, such as electrical, chemical, environmental and thermomechanical failure mechanisms. Examples of electrical failure mechanisms include electromagnetic interference, electrostatic discharge and electromigration. Examples of chemical failure mechanisms include corrosion, diffusion and dendritic growth. Environmental failures of electronic products can occur due to vibration, shock, humidity as well as radiation. The thermomechanical failure mechanism is the focus of this research. Thermomechanical failures are failures of electronic components and assemblies due to temperature loading conditions during manufacturing and service [2]. Figure 1.2 shows schematics of a flip chip package as well as a wire bond plastic ball grid array (WB-PBGA) package, which will be used to illustrate thermomechanical failure mechanisms. These two packages are commonly used in electronics manufacturing today.

Referring to Figure 1.2, thermomechanical failure mechanisms that can occur in a PWBA are delamination and warpage in the PWB and BGA substrate, delamination and fracture in the vias and copper traces, silicon die cracking, solder joint (ball) fatigue, fracture or opening, and delamination and voiding in the underfill or plastic molding. PWB and chip package warpage is the thermomechanical failure mechanism that will be studied in this research.

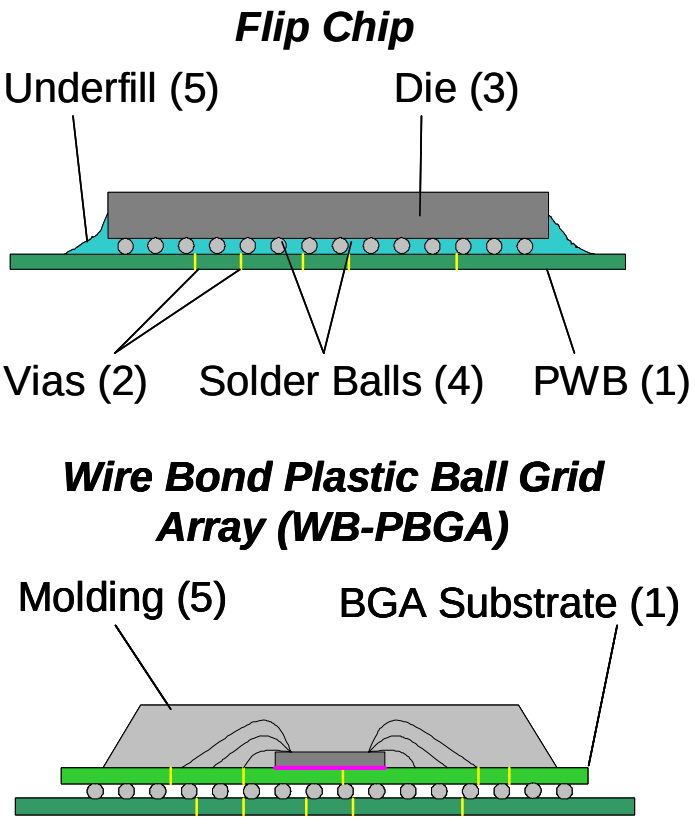


Figure 1.2. Flip chip and wire bond plastic ball grid array electronic packages

PWB/PWBA/chip package warpage investigation is important because during manufacturing, automated component placement or insertion is difficult or impossible in moderately or severely warped boards due to component misregistration. Also, board warpage is the major cause of electronic packaging reliability problems such as premature solder joint failure caused by high residual stress. The warpage problem in electronic packaging is a prevalent one and will continue to be a problem as the electronic packaging industry continues to move towards the manufacture of thin PWBs, high density PWBAs, miniature electronic components, and stacked dies and packages.

Several factors contribute to PWB warpage. A typical PWB consists of interposed layers of copper foil, with circuit traces, and dielectric materials (commonly FR-4) that are pressed and heated to form a laminate. During the lamination process, residual stresses develop in the PWB due to coefficient of thermal expansion (CTE) mismatch between the copper and FR-4 layers. In a PWBA, warpage can also be caused due to the CTE mismatch between the PWB and solder and between solder and the electronic components or die. Temperature loading conditions during PWBA manufacturing and field usage can also induce warpage in a PWBA. Figure 1.3 shows the surface mount

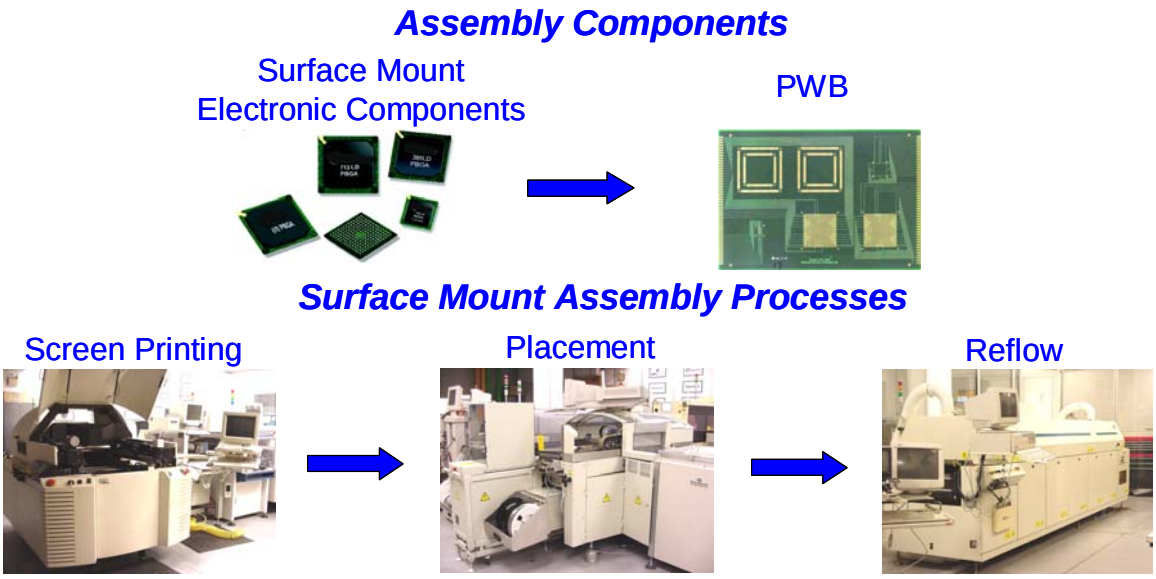


Figure 1.3. Surface mount assembly processes

assembly processes that are used to manufacture a PWBA. Figure 1.3 also shows the PWB and PBGA packages that will be used in this research. The main surface mount assembly processes are screen printing, chip package placement, and reflow. In the screen printing process, a stencil is placed over the PWB to be assembled. The stencil is custom manufactured for the PWB and has holes that line up exactly with the pads on the

PWB. Solder paste is applied to the stencil in order to the dispense solder paste onto the pads on the PWB. After the screen printing process, an automated chip package placement machine is used to place the chip packages onto their appropriate locations on the PWB. The chip package placement machine uses fiducial marks on the PWB as references in order to place the chip packages in the correct locations. After the placement process, the solder paste acts as a temporary glue to hold the chip packages onto the PWB. After the placement process, the chip packages are rigidly fixed to the PWB via a process called reflow soldering. PWB/PWBA/chip package warpage is a problem during the reflow soldering process. Many types of reflow processes are used in industry such infrared reflow, vapor-phase reflow, in-line conduction reflow, hot-bar reflow, laser reflow and forced convection reflow [3]. In addition to reflow soldering, wave soldering is currently used in industry for soldering leaded components and connectors to the PWB.

Infrared reflow employs infrared heating to heat the PWBA during reflow. Infrared heat is generated by heated IR emitter panels or elements which produce IR radiation in the near or far infrared range. The IR heater emitter panels and elements are located in the temperature zones of the infrared reflow oven. The temperature profile of the PWBA is determined by zone temperature and conveyor speed. The advantages of infrared reflow are that it provides for rapid heat transfer, and the equipment is inexpensive. The disadvantages of infrared reflow are that it has the tendency to heat the PWBA non-uniformly, due to the color sensitivity of infrared radiation and is difficult to profile for this very reason.

Vapor phase reflow involves heating a PWBA with the vapor of a fluorocarbon fluid which is boiled until it reaches the vapor state. The reflow soldering temperature is known and is the boiling point of the fluorocarbon fluid. A vapor phase reflow oven consists of a preheat zone containing IR emitter panels before the PWBA enters the vapor zone. The PWBA temperature profile is determined by the conveyor speed, the IR emitter panel settings as well as the vapor temperature. An advantage of vapor phase reflow is that it provides rapid uniform heating on a wide variety of thermal masses. A disadvantage of this reflow method is that the heat flow is too rapid and damages some components and materials due to thermal shock.

In-line conduction reflow involves heating the PWBA with a series of heated surfaces. The PWBA comes in direct contact with the heated surfaces, and is transferred from one surface to the next using a conveyor. The PWBA temperature profile is determined by the temperatures of the heated surfaces and the conveyor speed. The advantages of in-line conduction reflow are that it is easy to profile and is well suited for high temperature board materials such as ceramics. The disadvantages of inline-conduction reflow are that it is not well suited for epoxy boards and doesn't allow double-sided boards to be reflowed.

Hot-bar reflow consists of a resistance soldering device in which the electrode is made out of molybdenum through which an electric current is passed. The chip packages can be placed on solder paste or solder dipped to ensure that solder flows on the leads. The heat can be applied to the electrode either continuously or in a pulsed form.

Laser reflow consists of heating the chip packages to be soldered using a laser. It is ideal for heat sensitive PWBAs and densely packaged devices, since heat can be

applied to a localized area of the PWBA. A disadvantage is that if the laser energy is too high or if heat is applied for too short a time, a number of defects such as solder balling and charring may result.

Forced convection reflow is the predominantly used reflow method in industry. Forced convection reflow utilizes predominantly convective heating, even though an infrared heating component is always present. An advantage of convective heating is that it provides uniform heating and the slow heat transfer rate minimizes component cracking. A disadvantage is that convective heat transfer is slow, since the heater has to heat the gas and the gas has to heat the PWBA. Typical gases used are air and nitrogen. Nitrogen is sometimes used during reflow to reduce the formation of metal oxides. This reduces the work load of the flux, since the fluxing reaction involves removal of metal oxides. Industrial forced convection reflow ovens consist of 5 or 7 individually controlled temperature zones as shown in Figure 1.4, and the PWBA is heated from both the top and bottom sides of the oven [4]. Each zone is kept at a specific temperature, and the

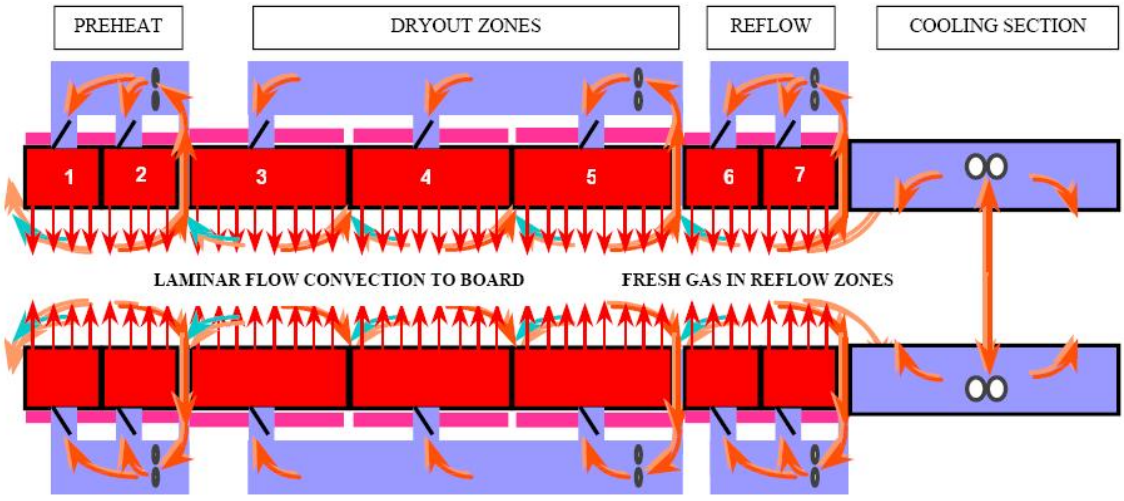


Figure 1.4. Schematic of 7 chamber convective reflow oven [4]

temperature profile is determined by the zone temperatures and the speed of the conveyor that the PWBA travels on.

During the reflow process, the PWB as well as the electronic components warp due to temperature loading and have the potential to cause reliability problems. Temperature loading conditions during field usage due to power cycling of the PWBA also contributes to PWB/PWBA/chip package warpage. In this research, PWBA warpage during the forced convection reflow process will be studied. In addition to CTE mismatch and temperature loading conditions, there are other factors that affect PWB/PWBA/chip package warpage such as PWB and chip package substrate thickness, Young's modulus of the PWB and chip package materials, temperature gradients through-the-thickness of the PWB/PWBA/chip package, chip package placement locations on the PWB and the PWB boundary constraints.

1.1 Research Objectives

In order to study PWBA warpage during the forced convection reflow process, several research objectives must be accomplished. The research objectives are:

I. To design and implement a forced convective heating warpage measurement system[*]. Forced convective heating enables the accurate simulation of forced convection reflow. The implemented forced convective heating subsystem will be automated and integrated with the current warpage measurement system.

II. To improve the software based digital image processing capability of the projection moiré warpage measurement system. Currently, the projection moiré system utilized

[*] The term "system" used in this dissertation refers to concepts for a subsystem, their combination and a specific implementation to test the concepts. It does not simply mean a machine.

at the Georgia Tech Advanced Electronic Packaging Laboratory (AEPL) is capable of capturing an image of PWB warpage. The system software for calculating the warpage across the surface of the PWB was designed for bare PWBs. The warpage across the surface of a bare PWB is the difference between the maximum PWB out-of-plane displacement and the minimum PWB out-of-plane displacement. When chip packages are present, the system software calculates an incorrect PWB warpage, because the maximum PWB out-of-plane displacement will be at the top of the tallest chip package on the PWB. The above problem will be corrected by developing an algorithm to automatically distinguish between the PWB and the chip packages, so that PWB warpage as well as chip package warpage can be calculated separately. A repeatability study will also be performed using the projection moiré warpage measurement system.

III. To utilize the improved projection moiré warpage measurement system to study PWBA test vehicle warpage. The test vehicle will consist of a PWB with up to two PBGA packages and will be used to study the effects of the chip packages on the warpage of the PWB during a convective heating process.

IV. To develop a finite element (FE) model technique to study PWB behavior with PBGA packages under thermal loading. The model will be used to study the effect of PBGA package locations on PWB warpage. Specifically, the FE model will enable the study of PWBA configurations not allowed by the available test vehicle.

After this introduction, literature relevant to the research objectives is reviewed in Chapter 2. The design of the convective heating system to simulate convective reflow is

presented in Chapter 3, and the development of a computational fluid dynamics model is to improve the performance of the convective system is included in Chapter 4. Chapter 5 discusses the development of the projection moiré measurement post-processing algorithm and presents projection moiré system performance results. Chapter 6 presents projection moiré warpage experiments to study the effects of PBGA packages on PWB warpage, and Chapter 7 presents the FE technique used to study the effects of PWBA chip package layout configurations on PWB warpage. Finally, conclusions, technical contributions and recommendations for future work are given in Chapter 8.

CHAPTER 2

LITERATURE REVIEW

Many researchers have studied the warpage of PWBs, PWBAs and chip packages. Before reviewing the work in the literature related to the study of warpage, an overview of the methods used to measure PWB/PWBA/Chip package warpage is presented below.

2.1 Warpage Measurement Methods

PWB/PWBA warpage can be measured by many different techniques such as the gauge indicator shim method, profilometry, interferometry and moiré methods. The gauge indicator shim method is fast, but ad-hoc in nature. The technique involves placing feeler gauges of different thicknesses under a PWB to determine PWB warpage. The gauge indicator shim method has poor accuracy, low resolution and cannot be used online.

There are two types of profilometry: contact profilometry and laser profilometry. Contact profilometry measures the surface profile of the sample by using a stylus that contacts the sample surface, and determines depth deflection of the stylus at each point on the sample with respect to a reference point. The advantage of contact profilometry is that it provides high resolution results. The disadvantages are that the stylus has to contact the sample surface and extensive two-dimensional scanning is required to understand the full-field topology which makes it unsuitable for online use [5, 6]. Laser profilometry measures the surface profile of the sample by using a laser that reflects from

the sample surface, and determines out-of-plane displacement based on the angle of the laser's reflection at each point on the sample with respect to a reference point. The advantages of laser profilometry are that it provides high resolution warpage results and it is a noncontact method. The disadvantage is that extensive two-dimensional scanning is required to understand the full-field topology which makes it unsuitable for online use [7].

Using interferometry, PWB warpage can be determined by splitting a continuous laser beam. One split beam acts as a reference. The other beam is reflected back from a PWB surface and is combined with the reference beam creating interference. The interference is due to the phase shift between the two beams. The interference pattern is used to determine PWB warpage. The most commonly used interferometry methods used are holographic interferometry, Twyman-Green interferometry and far infrared Fizeau interferometry. The difference between the interferometric methods lies in the optical setup, although the basic principles behind each method remain the same. The advantages of holographic interferometry are that it produces high resolution results and it is a noncontact method. The disadvantages of holographic interferometry are that it is very sensitive to noise, the optics are very complicated, both of which makes this method unsuitable for online use [8]. The advantages of Twyman-Green interferometry are that it produces very high resolution results and it is a non-contact method. The disadvantages of Twyman-Green interferometry are that the sample must have a mirror-like surface finish, the method can only be used to measure small samples such as flip chips, the optics are very complicated, and it is unsuitable for online use due to its limited sample applications [9, 10]. The advantages of far infrared Fizeau interferometry are that it

provides very high resolution results, it is a non-contact method and it can test optically rough surfaces. The disadvantages of far infrared Fizeau interferometry are that it can only be used to measure small samples such as flip chips, the optics are very complicated, and it is unsuitable for online use due to its limited sample applications [11, 12].

Moiré methods have emerged as the superior techniques for measuring warpage. Moiré methods are non-contact and full-field. The resolution of moiré methods is not as high as the resolution provided by interferometry, but the performance to cost ratio is much higher for moiré methods [13, 14, 15, 16, 17]. In this research, the projection moiré warpage measurement methods is used.

The shadow moiré technique is a non-contact, full field measurement method that generates a moiré fringe pattern. A moiré fringe pattern is a visual pattern that results

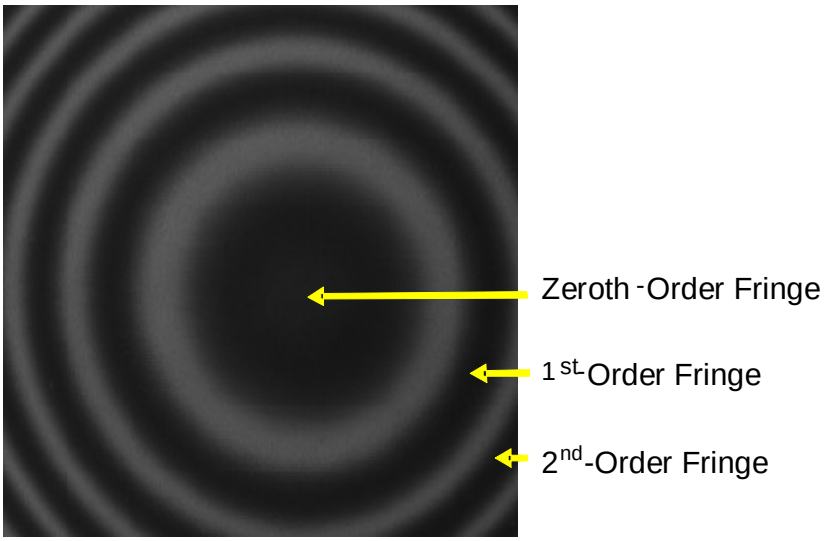


Figure 2.1. Moiré fringe pattern showing zeroth, first and second order fringes

from geometric interference between two periodic images. An example of a moiré fringe pattern is shown in Figure 2.1.

In a shadow moiré optical setup, as shown in Figure 2.2, one of the two periodic images comes from a glass grating. The other is the shadow of the grating lines created by diverging white light on a surface being measured. The glass grating is used as a reference. Small variations of the measured surface are magnified by moiré fringes and give a quantitative measure of surface topology. A CCD camera captures the moiré patterns and sends them to a computer to interpret out-of-plane displacement with respect to the reference grating. Precision motors connected to the sample holder provide better resolution and accuracy capability [16]. The resolution of the shadow moiré technique is equal to the pitch of the glass grating lines, when $\beta = 45^{o}$. As will be discussed below, the

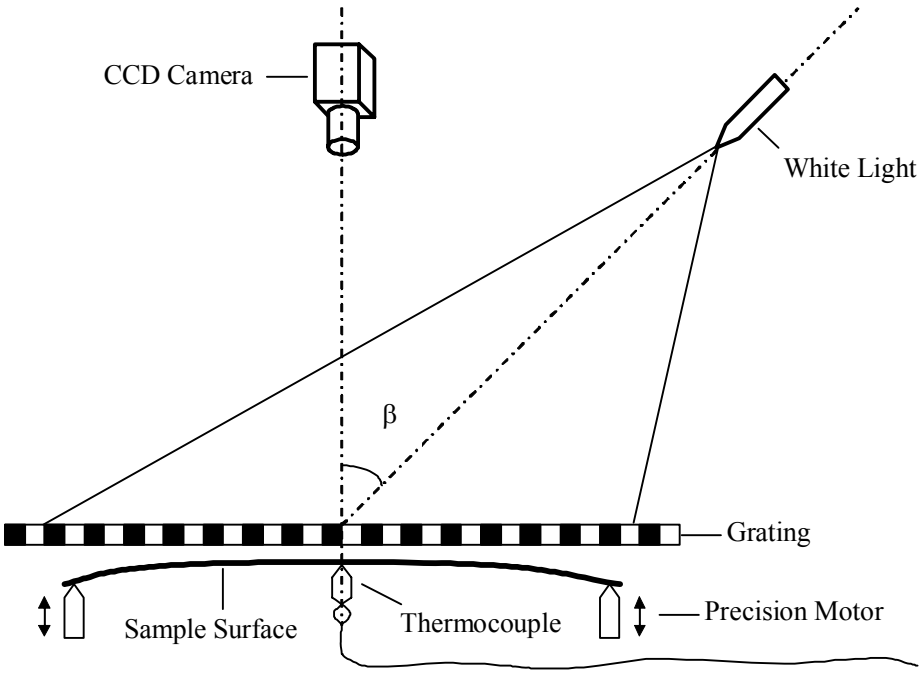


Figure 2.2. Shadow moiré optical setup

resolution can be increased to one hundredth of a grating pitch by a technique called phase stepping.

The projection moiré technique is also a non-contact, full field measurement method that generates a moiré fringe pattern. The major difference between the projection moiré technique and the shadow moiré technique is that the projection moiré technique uses a laser and an interferometer to generate parallel lines on the surface of the PWB/PWBA. No glass grating is required. As shown in Figure 2.3, the projection moiré optical setup consists of a laser, an interferometer, and beam redirection/expansion elements. A diode-pumped solid state laser, which has a wavelength of 532-nm is reflected and expanded before it enters a Michelson interferometer. The interferometer's reference mirror is mounted onto a piezoelectric transducer (PZT) for phase shifting to achieve high-resolution phase images. On the other side of the interferometer, there is an

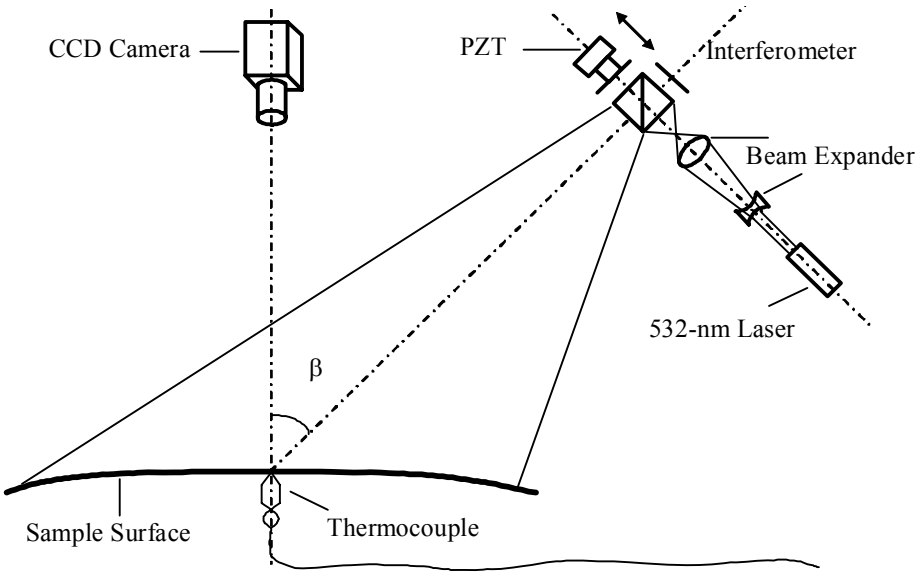


Figure 2.3. Projection moiré optical setup

adjustable mirror, which is controlled by two knobs. A CCD camera is used to record sample images. The CCD camera records two images in order to create a moiré fringe pattern. The first image, also called the reference grating pattern, is captured when the virtual grating lines are projected onto a flat reference surface. The second image is the deformed grating lines generated by a deformed sample surface. The moiré images are generated using software. The projection moiré system can also be used to measure relative warpage by capturing surface images before and after deformation [17]. The resolution of the projection moiré technique depends on the surface size being measured. Assume a sample with size L × L is under evaluation. Normally the 480 by 512 pixel CCD camera can resolve 100 fringes in its full field. Therefore, the resolution of the projection moiré measurement system is L/100. As will be discussed below, phase-stepping increases the resolution to L/10,000. The projection moiré system used in this research has high accuracy and has been shown to be capable of measuring out-of-plane displacements as small as 6 microns with 6.9 % accuracy.

The shadow moiré and projection moiré warpage measurement techniques are complementary to each other. For bare PWBs, the shadow moiré technique is the better choice due its high resolution, but for PWBs populated with electronic components, the projection moiré technique is better, because a glass grating is not required. The projection moiré technique is chosen for this research, because it can be used to measure populated boards and the technique does not require a glass grating that can interfere with convective heating processes.

For both the shadow moiré and the projection moiré warpage measurement systems described above, out-of-plane displacement, w, is calculated using Equation (2.1).

$$w = \frac{np}{\tan\alpha + \tan\beta} \tag{2.1}$$

where, n = fringe order

p = grating pitch

α = observation angle

β = illumination angle

For both the shadow moiré and projection moiré optical setups described above, the observation angle, α, is 0^o and the illumination angle, β, is 45^o. The fringe order, n, is determined from a moiré image. In the moiré image shown in Figure 2.1, the zeroth, first and second order fringes are labeled. Surface height difference between any two adjacent fringes on the moiré image is equal to the grating pitch since $\alpha = 0^o$ and $\beta = 45^o$. Therefore, the fringe order, n, can be determined by counting the fringes from the zeroth-order fringe on a moiré image. Note that the fringe order is not required to be an integer, and interpolation is required to obtain an accurate value. After the fringe order is determined, warpage can be calculated. Instead of using the fringe counting method described above to obtain the fringe order, a better technique called phase stepping can be used. Phase stepping produces a much more precise warpage result than the fringe counting method and typically increases the resolution of the warpage measurement by 100 times. Three-step and four-step phase stepping are the commonly used phase

stepping methods. The projection moiré measurement system used in this research employs four-step phase stepping. The PZT moves the reference mirror of the Michelson interferometer back and forth so that the phase of four moiré images is changed by π/2 consecutively as shown in Equation (2.2).

$$\varphi(x,y)=\arctan\left(\frac{I_{3(x,y)}-I_{1(x,y)}}{I_{0(x,y)}-I_{2(x,y)}}\right) \tag{2.2}$$

where, $\varphi(x,y)$ = moiré fringe phase

$I_i(x,y)$ = light intensity at pixel (x,y) for image i

After calculating the phase using Equation (2.2), Equation (2.3) is used to determine the fringe order, n.

$$n=\frac{\theta(x,y)}{2\pi} \tag{2.3}$$

where, $\theta(x,y)$ = moiré fringe phase value after φ(x,y) is made to vary between 0 and 2π (phase correction) and subsequently removing the 2π discontinuities (phase unwrapping).

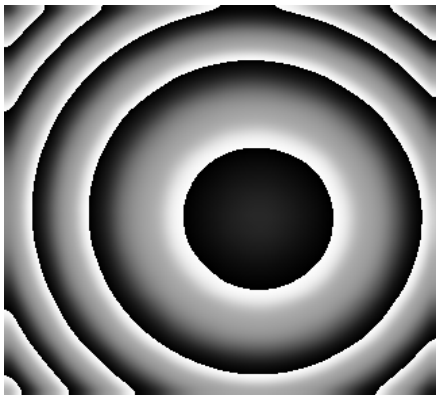


Figure 2.4. Wrapped phase image

The process of computing phase using phase stepped images such as in Equation (2.2) is called phase wrapping. Figure 2.4 shows the wrapped phase image corresponding to the moiré image in Figure 2.1. The $\varphi(x,y)$ term computed using Equation 2.2 will vary between $-\pi/2$ and $\pi/2$. In order for the correct fringe order, n, to be computed using Equation 2.3, the $\varphi(x,y)$ term must vary between 0 and 2π. The process of transforming the phase image to vary between 0 and 2π instead of varying between $-\pi/2$ and $\pi/2$ is called phase correction. The next step is to remove the 2π discontinuities which is called phase unwrapping. There are many different phase unwrapping methods available and advantages and disadvantages of each are discussed in Ding's dissertation [18].

After phase unwrapping, the out-of-plane displacement, w, calculated from Equation (2.1) is known at each point on the experimental PWB/PWBA/chip package sample. The out-of-plane displacement values can then be used to create an out-of-plane

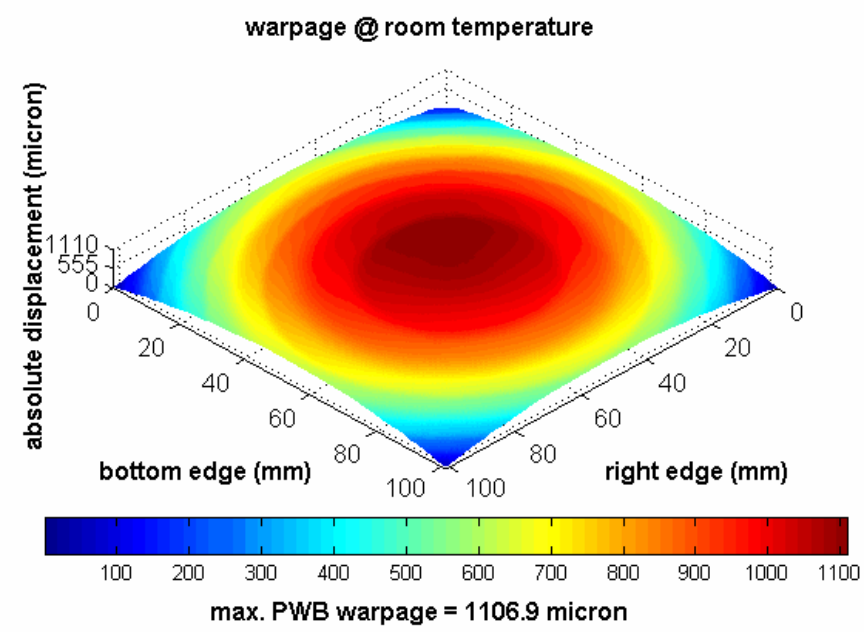


Figure 2.5. Example plot of out-of-displacement values for a PWB

displacement plot as shown in Figure 2.5. However, before the out-of-plane displacement plot is created, the out-of-plane displacement values must be rotated in order to obtain an accurate maximum warpage value. Maximum warpage of a PWB is calculated by taking the difference between the maximum and minimum out-of-plane displacements on the PWB. For this calculation, the out-of-plane displacements are referenced from the lowest point on the PWB in the out-of-plane direction. Maximum warpage of a PWBA is calculated by taking the difference between the maximum and minimum out-of-plane displacements on the PWBA. For this calculation, the out-of-plane displacements are referenced from the lowest point on the PWBA in the out-of-plane direction. In this dissertation, chip packages will be treated as a PWBA when calculating maximum chip package warpage. Maximum chip package warpage will be defined as the difference between the maximum and minimum out-of-plane displacements on the chip package. For this calculation, the out-of-plane displacements are referenced from the lowest point on the chip package in the out-of-plane direction, not including the solder

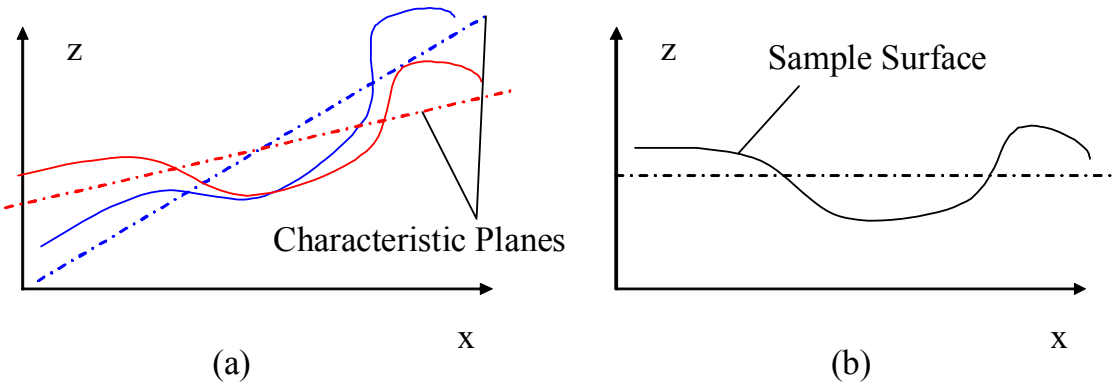


Figure 2.6. Surfaces before and after image rotation

joints. Rotation on the out-of-plane displacement values eliminates rigid-body rotation, and it allows maximum warpage comparison of differently oriented sample surfaces. As illustrated in Figure 2.6(a), the maximum warpage calculation is not unique when rigid-body-motion is present. When the characteristic plane of the surface is rotated to be horizontal as in Figure 2.6(b), a unique maximum warpage is identified. The characteristic plane can be calculated in several ways. One way is to use the least squares best-surface fit of the out-of-plane displacement values to represent the characteristic plane. After the characteristic plane is calculated, it is subtracted from the sample surface so that the characteristic plane becomes horizontal which in turns produces a unique maximum warpage result.

2.2 PWB/PWBA/Chip Package Warpage Study During Reflow Processes

The first objective of this research is to design and implement a forced convective heating warpage measurement system to simulate convective reflow. The developed system can then be used to measure PWB/PWBA/chip package warpage during convective reflow processes. Some researchers have published work studying warpage during reflow processes. Stiteler and Ume measured PWB warpage under a simulated wave soldering process demonstrating the usefulness of a novel warpage measurement system [19, 20]. Mittal et al. used FE analysis to study warpage of a surface mounted PWBA, consisting of J-leaded plastic leaded chip carriers (PLCCs) on an FR4 grade PWB during IR reflow soldering. The results showed that after reflow, the formed solder joints increased the stiffness of the PWBA. Also, the board warpage resulted in gaps at the lead-solder pad interface [21]. Polsky et al. studied the application of thermoelastic

lamination theory to predict PWB warpage with and without traces during thermal cycling and infrared reflow. An analytical model was developed. Warpage predicted by the model was compared to warpage measurements obtained using a shadow moiré technique. For the case of the PWB with traces, a micromechanics approach was used to develop quasi-homogenous effective representations of the trace layers. The results showed that the thermoelastic lamination theory model can be used to predict PWB warpage below the glass transistion temperature, T_g, of FR4. Above the T_g of FR4, viscoelastic relaxation may be present. Viscoelasticity was not accounted for in the model. The model was also not accurate at high temperatures, because temperature dependent CTE was not used [22, 23]. Polsky et al. compared PWB warpage due to simulated infrared and wave soldering processes. The results showed that PWBs heated using the simulated wave soldering process experienced higher warpage than boards heated using the simulated infrared soldering process. The discrepancy between the two processes was due to the significantly higher through-thickness temperature gradient experienced by the PWB during the simulated wave soldering process [24]. Wu et al. investigated the effects of rapid cure mold compound on warpage of PBGA packages using the shadow moiré technique during a simulated reflow process. The results showed that package warpage increased with mold compound curing time. The data also showed that a shorter reflow time resulted in smaller package warpage [25]. Djurovic et al. used FE analysis to study thermally induced warpage of a PWBA with an array of pin-through-hole (PTH) connectors during a dual-wave soldering process. A sensitivity analysis was performed to study the effects of varying material properties on the warpage of the assembly [26]. The results showed that the overall assembly warpage was most

sensitive to the CTE of the PWB and connector. Muncy et al. investigated the warpage of a flip chip assembly using the shadow moiré technique during simulated infrared solder reflow in order to optimize the reflow profile. The results aided in the development of a robust reflow process that resulted in yields of 98% or greater [27]. Ding et al. also studied the warpage of a flip chip assembly during a simulated infrared reflow process and found that the warpage of the assembly decreased after reflow and then increased after underfill application [28]. The major gap in the previous research studying warpage during reflow processes is that previous research presented warpage studies using FE modeling or infrared reflow processes. Infrared reflow processes induce large temperature gradients that can affect the accuracy of warpage studies. As discussed in Chapter 1, forced convective reflow is the dominant type of reflow currently used in industry. In order to study PWB/PWBA/chip package warpage during convective reflow processes, a system capable of simulating convective reflow while simultaneously monitoring warpage must be developed.

2.3 PWB/PWBA/Chip Package Warpage Study Using the Projection Moiré Technique

The second objective of this research is to develop and implement a post-processing algorithm for the projection moiré system that enables simultaneous calculation of PWB and chip package warpage from a PWBA warpage measurement. Some work has been published using the projection moiré technique to measure warpage. Daniel et al. studied room temperature warpage of laminates that are symmetric and antisymmetric about their midplane with different stacking sequences and found that

symmetric laminates warp either concave up or concave down, while antisymmetric laminates tend to warp into a saddle shape. Warpage measurements using a projection moiré technique were compared to analytical lamination theory warpage calculations. The results showed that laminate stacking sequence does not account for all of the warpage. Other factors should be considered such as laminate processing conditions [29, 30, 31]. Wang et al. used linear viscoelastic theory along with classical lamination theory to predict residual stresses and warpage in multidirectional woven-glass/epoxy laminates. The predicted warpage results agreed favorably with warpage measurements obtained using a projection moiré method [32]. He et al. used a PBGA package as a measurement application to demonstrate a real-time warpage measurement system using the projected grating method and showed that the system could provide a high resolution warpage measurement [33]. Ding et al. compared the projection moiré and shadow moiré measurement techniques at room temperature and found that the two measurement techniques complement each other. A high quality warpage measurement system should incorporate both measurement techniques [16]. Ding et al. also used the projection moiré technique to study the warpage of PWBAs such as a computer motherboard and a module from a communication base station product to demonstrate the capability of a novel projection moiré measurement system [17]. Apart from the projection moiré system used in this research, other systems are limited to measuring small samples. The projection moiré system used in this research can measure various sample sizes, and populated boards, but is currently unable to distinguish between the maximum warpage of the PWB and the maximum warpage of chip packages. Therefore, an algorithm will be developed

to solve this problem. Also, a repeatability study will be performed on the projection moiré warpage measurement system.

2.4 Experimental Study of PWB/PWBA/Chip Package Warpage

In addition to the literature reviewed in the previous sections, other significant work has been done to experimentally study PWB/PWBA/chip package warpage. Petriccione and Ume studied the effects of moisture and gradual heating on warpage of high density interconnect (HDI) PWBs using the shadow moiré technique. The results showed that moisture has an effect on warpage and that thicker HDI boards experience less warpage than their thinner counterparts [34].

Dang, Ume and Bhattacharya performed numerous studies on the warpage of substrates for large area multi-chip module-deposited (MCM-D) packaging. Warpage measurement studies were performed on flexible stainless steel substrates, dielectric coated stainless steel substrates, multitiled alumina substrates, multitiled silicon substrates and conductive gallium alloy via-filled stainless steel substrates using the shadow moiré technique. For the flexible stainless steel substrates, the warpage results showed that the overall substrate warpage reduced after dielectric coating and via filling and that after thermal cycling, larger MCM-D modules resulted in smaller warpage values. For both the multitiled alumina and multitiled silicon substrates, the warpage of the tiles and pallet assembly used in the study increased after the curing process. Also, the results showed that polishing reduced the overall warpage of the initial pallets [35, 36, 37, 38].

Banerji et al. studied the effect of substrate warpage on next generation high-density wiring requirements and found that stiff substrates are necessary in order to meet the requirements [39]. Bansal et al. studied warpage of low CTE, high stiffness organic and inorganic boards for flip chip on board applications without underfill using the shadow moiré technique. Stress measurements were also taken and correlated with failures such as dielectric cracking and delamination. The results showed that substrates should have high stiffness in addition to low CTE for reliability of flip chip on board applications without underfill [40, 41]. Han et al. studied the warpage of PWBs with various surface mount components using the shadow moiré technique with enhanced sensitivity. The results showed that the technique can only be used to measure local warpage and not global warpage of PWBAs [42]. J. Zhang et al. used the shadow moiré technique to characterize substrate warpage during assembly of a flip chip assembly on warped organic substrate [43]. Ham and Lee studied the assembly warpage during heating of a wafer level CSP assembly using moiré interferometry and found that nonlinear thermal deformations during heating were caused by creep and stress relaxation of the solder joints [44]. Wang and Hassell used the shadow moiré technique to measure the thermally induced warpage of PBGA packages and compared the warpage of the package to the warpage of the substrate at the location of the PBGA package [45, 46]. Shook et al. studied the effects of ingressed moisture on warpage of PBGA packages. The results showed that with increased moisture, warpage of the PBGA increases and solder joint failures also increase [47]. S. Wu et al. used the shadow moiré technique to measure thermally induced warpage of a populated BGA panel to investigate material behavior on BGA quality [48]. Liang studied the effect of substrate thickness, package assembly

process, die size, encapsulation thickness and size on warpage of an enhanced PBGA (EPBGA) package. The results showed that encapsulation thickness was the most significant factor on package warpage, with smaller encapsulation thicknesses resulting in higher warpage. The data also showed that maximizing the substrate thickness and minimizing the encapsulation size could reduce the impact of encapsulation height on package warpage [49]. Wang et al. used the shadow moiré technique to compare warpage of PBGA packages induced by thermal cycles after different types of slots were machined into the encapsulation molding. The results showed that the machined slots significantly improved PBGA package warpage induced by thermal cycles [50].

The literature presented above shows that significant experimental warpage studies have been conducted. However, no full-field measurement studies on populated PWBs have been conducted. This research will fill this gap by studying the effect of PBGA packages on PWB warpage during a convective heating process.

2.5 Finite Element Modeling to Study PWB/PWBA/Chip Package Warpage

The third objective of this research is to develop a FE technique to study the warpage of PWBs with PBGA packages. Several researchers have published work using FE analysis to study warpage. In addition to the work presented in previous sections, Yeh and Ume et al. investigated many different analytical and experimental approaches to determine thermally induced PWB warpage. The shadow moiré technique was determined to be the best method to measure warpage. Sensitivity analyses were also conducted using FE analysis in order to determine which PWB material properties had significant effects on thermally induced PWB warpage. The results showed that CTE was

the most influential material property followed by Young's modulus and layer thickness [13, 14]. Fu and Ume characterized temperature dependence of PWB material properties, and then used the properties and FE analysis to predict PWB warpage during heating processes. The FE analysis model was also compared to shadow moiré experimental results to show the importance of using temperature dependent properties [51]. Ume et al. studied PWB warpage due to the solder masking process using FE analysis. The study showed that using solder mask thicker than 1.1 mils resulted in lower warpage. Also, better warpage results were obtained when solder mask of the same thickness was applied to both sides of the PWB. A sensitivity analysis was also performed to determine which solder mask material properties had the greatest effect on PWB warpage. The sensitivity analysis showed that CTE of the solder mask had the greatest effect on PWB warpage followed by Young's modulus and Poisson's ratio. The analysis also showed that the influential properties affected thinner PWBs more than thicker PWBs [52, 53]. Dunne and Sitaraman developed a process modeling methodology that enables monitoring of warpage and stresses during sequential multilayered substrate fabrication. Shadow moiré experimental results were used to validate the model. The results demonstrated the importance of incorporating viscoelasticity into the model in order to accurately predict the warpage of the substrate [54]. Ding et al. developed a FE modeling methodology for predicting PWBA warpage. The modeling methodology utilizes modularized, parametric and effective modeling schemes [55]. Ding et al. used FE analysis to study the effects of several parameters on PWBA warpage. The results showed that FR-4 Young's modulus, temperature variation and PWB thickness were the most influential parameters [56]. Yao and Qu studied the effect of PWB size on the warpage of flip chip assemblies using FE

analysis and found that PWB size has very little effect on the overall flip chip assembly warpage [57]. Yang et al. used FE analysis to study the effect of ribbed package geometry on the thermal warpage of a PBGA. The study showed that thermal warpage can be significantly reduced if the thickness, width and Young's modulus of the rib is appropriately selected [58]. Moore et al. used FE analysis to study the warpage of PBGA packages and found that the orientation and density of copper traces on the bismaleimide triazine (BT) substrate has a significant effect on BT substrate warpage [59]. Teng et al. studied the impact of polymerization on warpage prediction of molded plastic packages. A profilometer was used to measure package warpage and to validate an FE model. The results showed that the degree of polymerization of the mold in electronic packages should be taken into account in order to accurately predict package warpage [7]. Yeung et al. used three dimensional FE elastic and viscoelastic models to predict warpage of PQFPs and found that the viscoelastic model was more accurate than the linear elastic model. The FE models were validated using profilometry [4]. Tee et al. studied block BGA warpage using FE analysis and surface profilometry and found that lower mold compound CTE and modulus are preferred for lower warpage. Also, mold compound with high T_g and lower chemical shrinkage also helps to reduce warpage. Block warpage is also reduced with a thicker substrate [6]. Li et al. used FE analysis to study the warpage of flip chip PBGA packages and found warpage decreases with higher CTE and modulus of the heat spreader as well as more contacting area between the heat spreader and the substrate. PBGA warpage also decreases with die thickness and decreases with a thermal interface material with good adhesion and high modulus. Li et al. also found that warpage increases with die size and package size [60]. Chong et al. investigated the

warpage of fine-pitch BGA (FBGA) packages and found that package warpage increases with substrate thickness, die thickness and package size to die size ratio [61]. Verma et al. used FE analysis, the shadow moiré method and far infrared Fizeau interferometry to study thermally induced warpage of a flip chip PBGA package. A parametric study was conducted to identify the factors critical to solder joint reliability. The authors found that substrate CTE was the most critical factor [12]. Xie et al. used FE analysis to investigate board level drop for handheld devices and found that board warpage increases when the board is constrained in a fixture resulting in lower reliability [62]. Amagai et. al studied the reliability of chip scale PBGA packages and found that solder joint reliability decreases with increasing warpage. As the molding compound CTE and modulus increases, solder joint reliability decreases due to increased warpage. Solder joint reliability also decreases with decreasing T_g [63]. Zhang et al. developed an advanced warpage prediction methodology for matrix stacked die BGAs and found that crossbow dominant warpage and buckling phenomena are observed for the matrix after bottom die bonding and after interposer bonding. Also, total die length as well as dice distribution also affects the warpage pattern of the matrix [64]. Zwemer et al. and Bajaj et al. perfomed research on automating bare board simulations using standards-based ECAD models. The results showed that the methodology is capable of investigating warpage at the local feature level as well as the global PWB/PWBA level. Models were validated with moiré experimental results [65, 66]. Recently, Peak et al. successfully performed research on automating assembled board simulations using standards-based ECAD models and validated the results using projection moiré experiments. Peak's research allows efficient introduction of detailed feature information into warpage models of

varying fidelity [67]. Zeng et al. and Zeng successfully used information-based FEA models to study chip package deformation or warpage [68, 69].

The literature presented above show that significant warpage studies have been conducting using FE analysis. However, the effects of chip package placement on assembly warpage during convective reflow have not been studied. In this research, an FE model technique is developed do study the warpage of PWBs populated with PBGA packages during convective reflow.

CHAPTER 3

DESIGN AND DEVELOPMENT OF A CONVECTIVE REFLOW SYSTEM FOR WARPAGE METROLOGY

3.1 Convective Heating System Requirements

In order to simulate convective reflow, it is necessary to have an oven that has a forced convective heating capability. The first objective of this research is to design and implement a forced convective heating subsystem to be used with the existing warpage measurement system. Figure 3.1 shows the initial oven configuration before this research

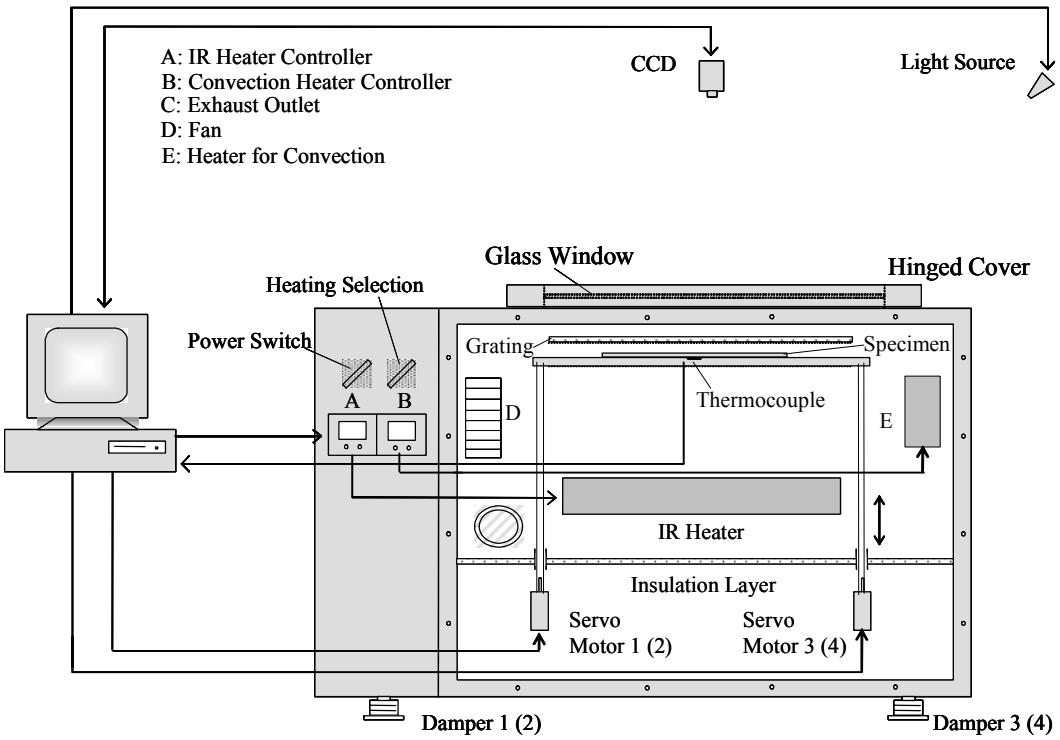


Figure 3.1. Warpage measurement system (only the shadow moiré optics are shown)

project was undertaken. Only the shadow moiré optics are shown. The previous warpage measurement system was capable of measuring PWB/PWBA warpage during thermal infrared (IR) heating. To demonstrate the disadvantage of this method, infrared heating was used to heat a 203.2 mm by 139.7 mm by 0.631 mm PWB from room temperature to 220 ^{o}C, which is within the peak reflow temperature range for assemblies using eutectic solder. Figure 3.2 shows the thermocouple placement locations on the PWB.

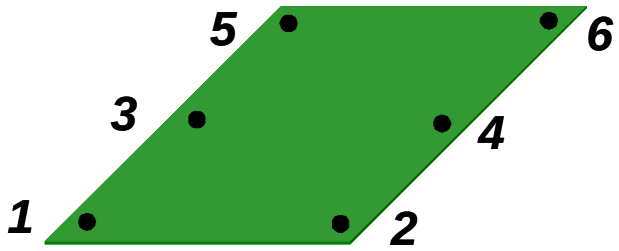


Figure 3.2. Thermocouple placement locations on a 203.2 mm by 139.7 mm by 0.631 mm PWB

At each of the 6 locations shown in Figure 3.2, thermocouples were placed on both the top and bottom sides of the PWB for a total of 12 thermocouples. Figure 3.3 shows temperature versus time curves for each of the thermocouples during the infrared heating experiment. Figure 3.3 shows that a significant temperature difference exists through-the-thickness of the PWB. Table 3.1 shows the through-the-thickness temperature difference at each thermocouple placement location. Table 3.1 shows that the PWB through-the-thickness temperature differences range from 31.3 ^{o}C at location 1 to 41.6 ^{o}C at location 4. A large temperature difference through-the-thickness of the PWB causes warpage,

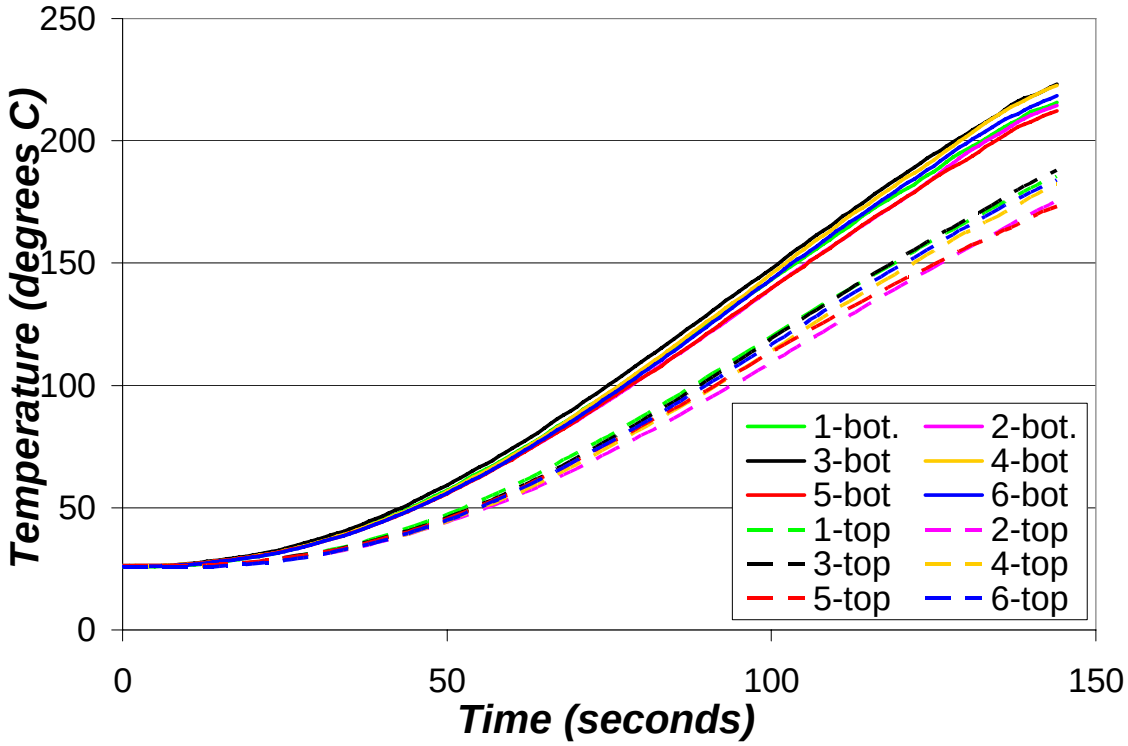


Figure 3.3. Temperature vs. time curves at four locations on a 203.2 mm by 139.7 mm by 0.631 mm PWB during infrared heating

Table 3.1. Maximum PWB through-the-thickness temperature difference during infrared heating

PWB Thermocouple Locations	1	2	3	4	5	6
Maximum PWB Through-The-Thickness Temperature Difference during Infrared Heating (^{o}C)	31.3	40.4	36.3	41.6	39.9	35.5

therefore, in order to reduce the level of warpage caused by reflow process, the PWB through-the-thickness temperature difference must be minimized. The average maximum through-the- thickness temperature difference of 41.6 ^{o}C will be used as a baseline to compare the convective heating system to the infrared heating system. In order to simulate convective reflow accurately, the convective heating system should be able to follow reflow profiles. Figure 3.4 shows an example of the most commonly used

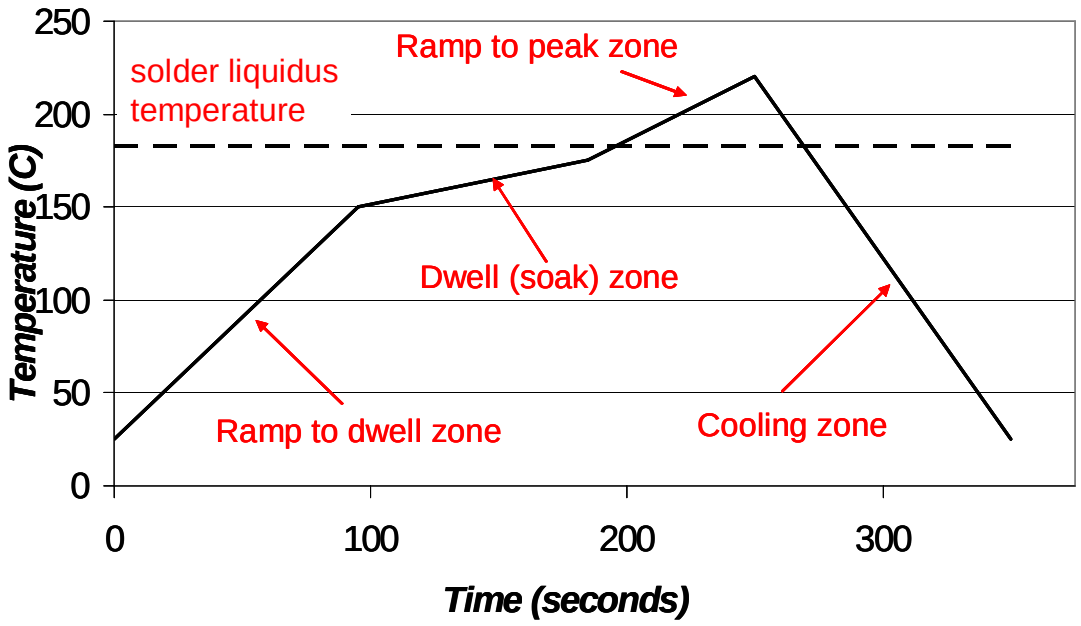


Figure 3.4. Typical ramp to dwell, ramp to peak reflow profile

reflow profile which is the ramp to dwell, ramp to peak (RDRP) profile. The RDRP profile consists of four zones: the ramp to dwell zone, the dwell or soak zone, the ramp to peak zone and the cooling zone. Many component manufacturers specify a maximum rate of temperature rise of 2 to 4 ^{o}C/second in the ramp to dwell stage of the reflow

profile [3]. Typically, a maximum ramp rate of 2 ^{o}C/second is used, because higher ramp rates may result in thermal shock to the assembly components. The purpose of the dwell (soak) zone is to evaporate solvents and activate the flux in the solder paste as well as to allow the assembly to reach a uniform temperature before entering the reflow zone. In the ramp to peak zone, the assembly is heated above the solder liquidus temperature to a peak temperature, typically between 200 to 225 ^{o}C which allows the solder to melt completely. During this zone, a minimum dwell time above liquidus is usually specified. Subsequently, the assembly is cooled to room temperature. Figure 3.5 shows another type of reflow profile which was recently developed by Lee [5]. Lee optimized the reflow profile using defect mechanisms analyses and found that for forced convective reflow ovens, the optimized reflow profile consists of a slow ramp (approx.

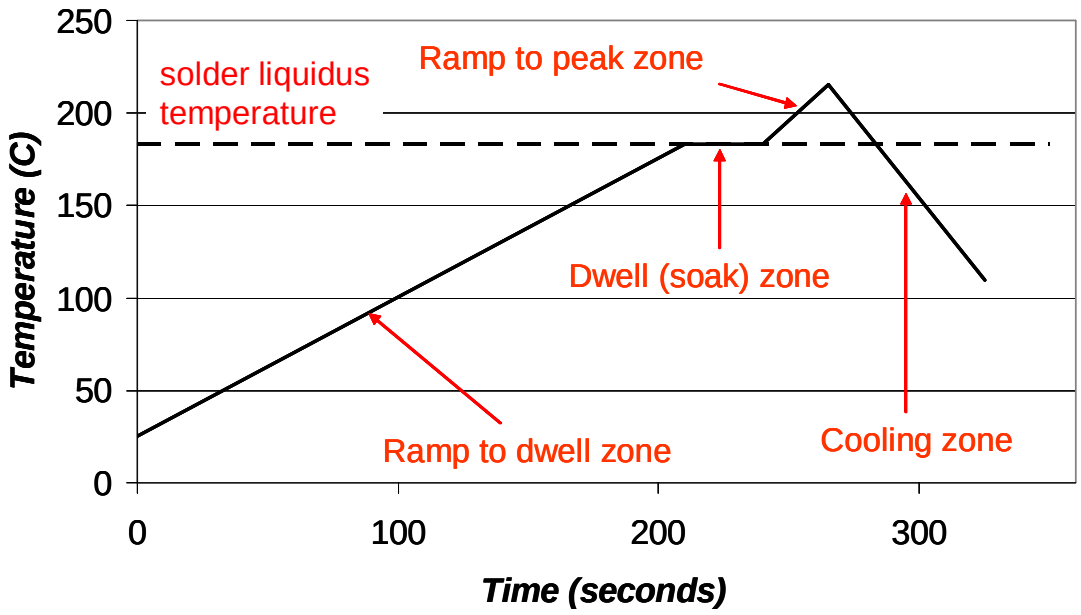


Figure 3.5. Lee optimized reflow profile

0.5 – 1.0 ^{o}C/second) to the solder liquidus temperature, a short dwell at the solder liquidus temperature followed by a ramp to the peak reflow temperature. In order to simulate reflow accurately, the convective system designed for this research should be capable of following reflow profiles such as the ones shown in Figure 3.4 and Figure 3.5. This is a difficult task, since the temperature of the single oven chamber must be varied continuously. As mentioned earlier, industrial reflow ovens enable the PWB/PWBA to follow the reflow temperature profile by passing it through multiple heating chambers which are kept at constant temperatures.

3.2 Original Convective Heating System Configuration

Before this research project was undertaken, there was an existing convective heating system. There were several problems with the existing design. The first problem was the heating element selected for convective heating. The heating element used for convection was a 3750 W panel heater with a heat density of 7750 W/m^2. The main problem with the heater was its slow heat-up rate. In order to demonstrate the slow PWB heating due to the initial convection design, the heating element was used to heat a 76.2 mm by 76.2 mm by 0.6 mm PWB from room temperature to 85 ^{o}C. A thermocouple used to monitor the PWB temperature was placed on the bottom of the PWB. Figure 3.6 shows the temperature versus time plot that resulted from this experiment. Figure 3.6 shows that for the initial convective heating system, the PWB took over one hour to be heated from room temperature (25 ^{o}C) to 85 ^{o}C. If the PWB temperature vs. time plot is assumed to be linear, then the heating rate of the PWB can be obtained by taking the slope of the

measured temperature profile in the Figure 3.6. This results in a PWB heat up rate of 0.016 ^{o}C/s, which is very far off the target PWB heat up rate of 2 ^{o}C/s.

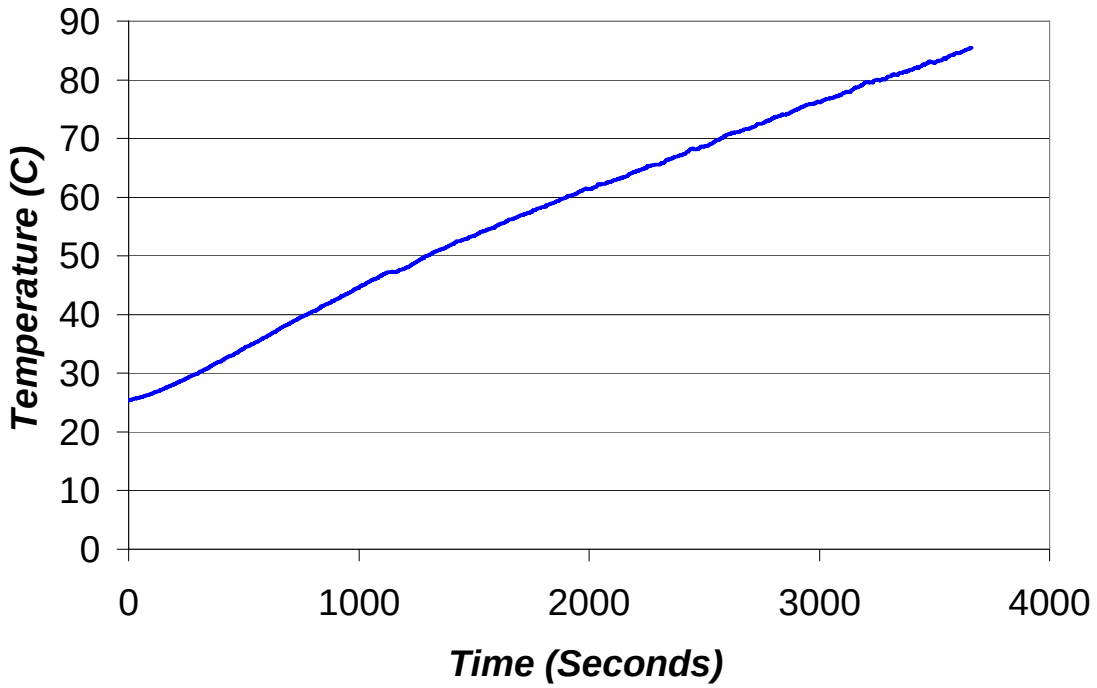


Figure 3.6. Temperature vs. time curve at one location on a 76.2 mm by 76.2 mm by 0.6 mm PWB during convective heating from room temperature to 85^{o}C

Another problem with the initial convective heating system was airflow path design. Figure 3.7 below shows a top view schematic of the oven chamber showing the airflow path through the oven. Figure 3.7 shows the PWB in the center of the oven chamber. A centrifugal fan, shown at the left side of the oven chamber, draws air from the oven chamber and redirects it into a 101.6 mm by 228.6 mm channel. The air then makes a 90-degree turn into a 25.4 mm by 228.6 mm channel where it flows to the right side of the oven. The air then makes a 180-degree turn and flows across the heater and back into the oven chamber and the cycle repeats. The major problem with this design

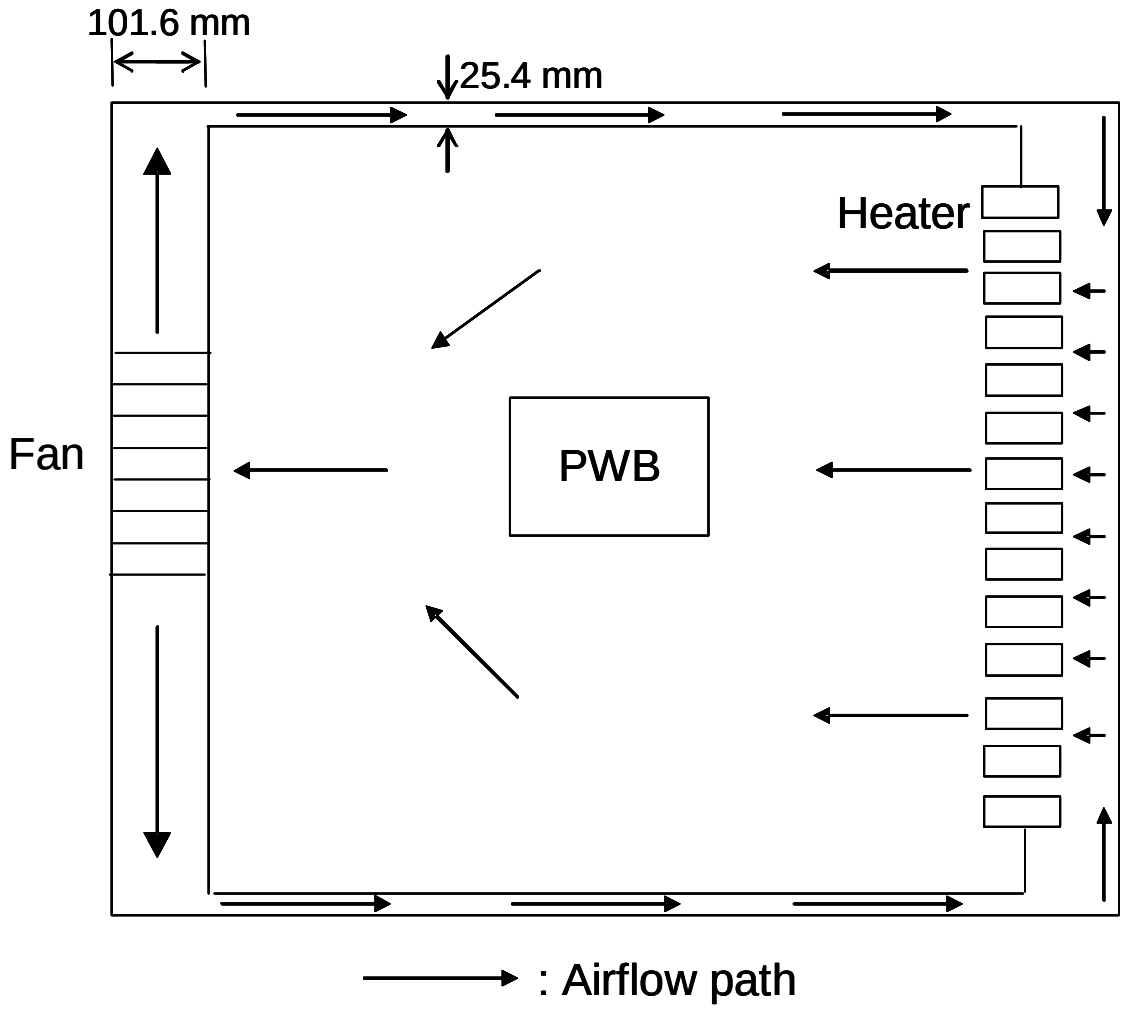


Figure 3.7. Top view schematic showing original convection system airflow path

was that little or no air was getting directed into the 25.4 mm by 228.6 mm channels. This resulted in very low airflow across the heater. Airflow measurements were taken directly in front of the heater using a hand-held air velocity indicator. The air velocity in front of the heater ranged between 0.0762 m/s and 0.1524 m/s, which resulted in approximately no airflow over the PWB surface. Another problem with the initial design was that the fan was bolted directly to the oven, so vibrations from the fan interfered with moiré warpage measurements, which are vibration sensitive. In addition, the speed of the fan could not be varied. Therefore, the initial convective system configuration provided no means to optimize the heating process by adjusting air velocity. After the initial convective heating system design was evaluated, a complete redesign was performed. The redesigned convective heating system is discussed next.

3.3 Redesigned Convective Heating System

The convective reflow warpage measurement system designed in this research is shown in Figure 3.8. The system is capable of measuring the warpage of PWBs/PWBAs/chip packages using the shadow moiré and projection moiré techniques. The oven in Figure 3.8 is used for dynamic warpage measurement during infrared and convective heating processes. The shortcoming of using infrared heating processes during warpage measurements was discussed earlier. In addition to the oven chamber, the convective heating system consists of 12 tubular heaters totaling 36 KW and a 1250 CFM centrifugal fan, which is controlled using a variable frequency drive. The tubular heaters and the fan were placed on the right side of the oven chamber due to space constraints. Since both the shadow moiré and projection moiré warpage measurement techniques are

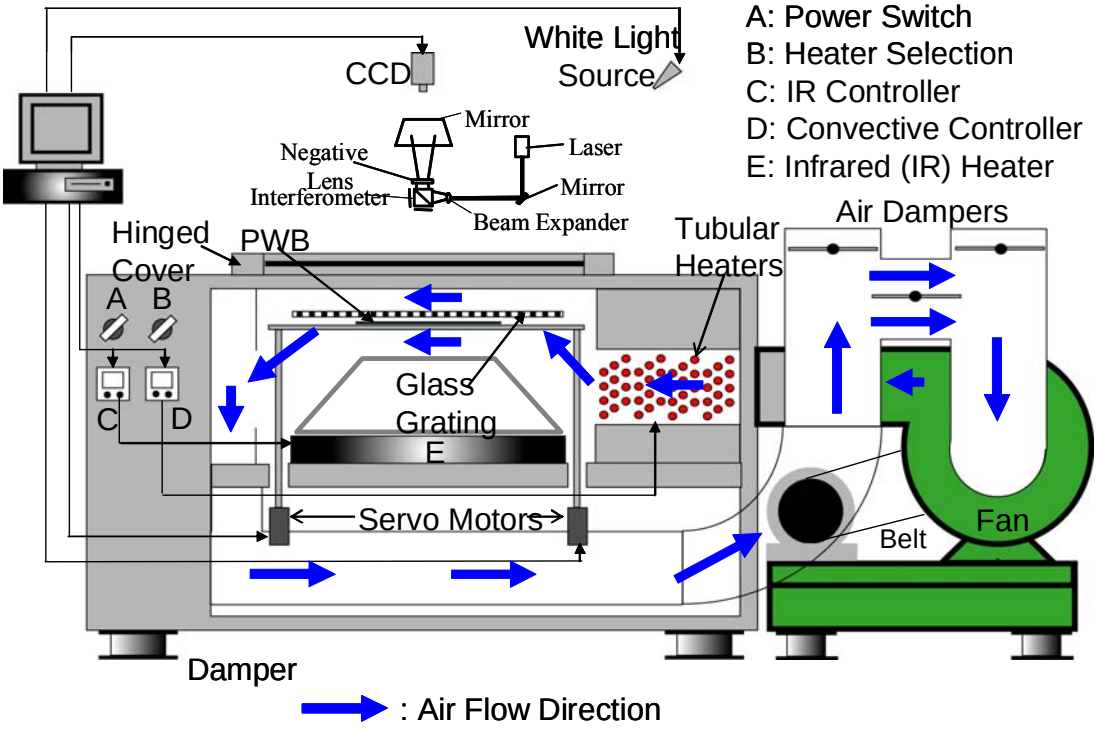


Figure 3.8. Schematic of warpage measurement system to simulate convective reflow

sensitive to vibration, the oven and fan are both mounted on vibration isolators. The fan is connected to the oven using a flexible duct. Air dampers are used to control the flow of air through the system. When the two upper air dampers are in the closed position as in Figure 3.8, the lower air damper is in the open position and air recirculates through the system. When the two upper air dampers are in the open position, the lower air damper is in the closed position, and fresh air is drawn from the room through the right vertical duct while air is expelled from the system through the left vertical duct. This mode is used for cooling PWB/PWBA/chip package samples. A temperature controller is used to control the tubular heaters via a PC.

The 1st Law of Thermodynamics was used to estimate the ideal heating rate of the total volume of air in the system with a heat input of 36 kW. The calculation is shown below.

For a control mass (closed system on a time rate basis), the total energy rate is given by Equation (3.1).

$$\frac{dE}{dt} = \dot{Q}_{in} - \dot{W}_{out} \tag{3.1}$$

where,

dE/dt = total energy rate (W)

$\dot{Q}_{in}$ = energy input to the system per unit time (W)

$\dot{W}_{out}$ = work output from the system per unit time (W)

The total energy rate can be expressed by Equation (3.2).

$$\frac{dE}{dt} = \frac{d}{dt}\int \rho e \, dV \tag{3.2}$$

where,

e = total energy (J/kg)

The total energy, e, can also be expressed as Equation (3.3).

$$e = u + ke + pe \tag{3.3}$$

where,

e = total energy (J/kg)

u = internal energy (J/kg)

ke = kinetic energy (J/kg)

pe = potential energy (J/kg)

In terms of continuously varying local properties,

$$\frac{d}{dt}\int \rho e\, dV = \frac{d}{dt}\int \rho(u+ke+pe)\, dV = \dot{Q}_{in} - \dot{W}_{out}$$

Since there is no kinetic energy, potential energy or work output for this problem,

$$\frac{d}{dt}\int \rho(u)\, dV = \dot{Q}_{in}$$

Assuming constant volume,

$$\frac{d(\rho u V)}{dt} = \dot{Q}_{in}$$

$$\rho V \frac{du}{dt} = \dot{Q}_{in}$$

Since $u = c_v T$,

$$\rho V \frac{d(c_v T)}{dt} = \dot{Q}_{in}$$

$$\rho V c_v \frac{dT}{dt} = \dot{Q}_{in}$$

$$\frac{dT}{dt} = \frac{\dot{Q}_{in}}{\rho V c_v}$$

For air, ρ = 1.1614 kg/m^3 at 300K

c_p = 1.007 kJ/kg K at 300K

$c_v = c_p - R$ =1.007 kJ/kg K – 0.287 kJ/kg K

= 0.72 kJ/kg K

For the convective heating system, V = 0.39 m^3.

Therefore,

$$\frac{dT}{dt} = \frac{36\,kW}{(1.1614\,kg/m^3)(0.39\,m^3)(0.72\,kJ/kg\,K)} = 110.4\ K/s$$

An ideal air heating rate of 110.4 ^oC/second is promising, since it is significantly higher than the desired system heating rate of 2 ^oC/second. However, the actual system heating rate should be expected to be much lower due to heating and flow losses. The measured performance of the convective heating system is discussed next.

3.4 Convective Heating System Performance

The performance of the convective heating system was evaluated by using it to heat a 203.2 mm by 139.7 mm by 0.631 mm PWB from room temperature to 220 ^oC. Twelve thermocouples were placed on the PWB in the same configuration shown in Figure 3.2. Exploratory experiments were conducted to determine the optimum air velocity for the convective heating system. The experiments were conducted by varying the frequency of the fan between 20 Hz and 30 Hz. There is a linear relationship between fan frequency and air velocity at the fan outlet as shown in Figure 3.9. Figure 3.9 below shows the relationship between air velocity at the fan outlet and fan frequency. Figure 3.9 shows that the fan outlet air velocity follows a linear trend with respect to fan frequency which is expected. The regression equation can be used to set fan frequencies for desired outlet air velocities between 0 and 22.5 m/s. A lower bound of 20 Hz was

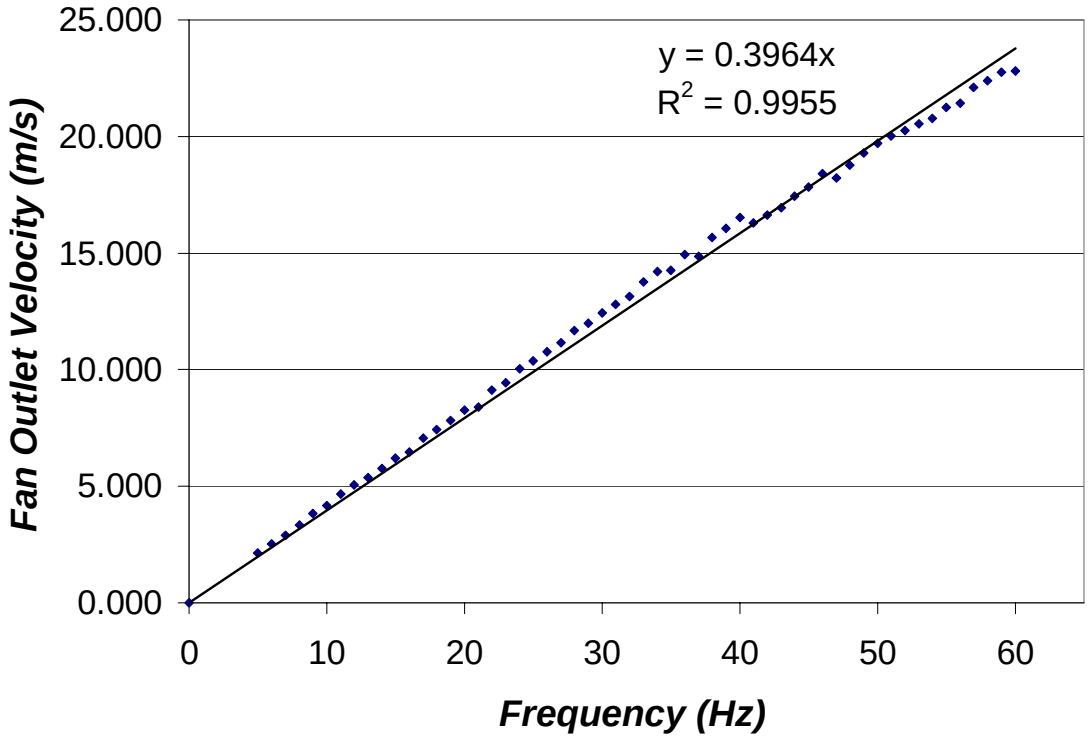


Figure 3.9. Fan outlet velocity versus fan frequency

chosen to prevent tubular heater damage due to insufficient airflow across the heaters as recommended by the heater manufacturer. An upper bound of 30 Hz was chosen, because above 30 Hz, the fast airflow causes the PWB/PWBA sample to vibrate which affects shadow moiré and projection moiré warpage results. Table 3.2 below shows PWB heating rates which were calculated from the experimental temperature data at each frequency of the fan.

The PWB heating rates shown in Table 3.2 were calculated by using an average heating rate for each of the 12 PWB thermocouple locations and subsequently averaging the 12 heating rates to obtain one metric to compare all fan frequencies used in the experiment. A general trend can be observed from Table 3.2. At fan frequencies from 20

to 23 Hz, the PWB heating rate is approximately 0.55 ^{o}C/second and higher. At fan frequencies 24 Hz and higher, the PWB heating rate decreases significantly all the way down to approximately 0.47 ^{o}C/second at a fan frequency of 30 Hz. The same trend was observed with three replicates of the experiment. Twenty three Hertz was chosen as the optimum fan frequency, because it is the highest frequency just before which the

Table 3.2. Average temperature rate versus fan frequency for a 203.2 mm by 139.7 mm by 0.631 mm PWB during convective heating

Fan Frequency (Hz)	Average PWB Temperature Rate (^{o}C/s)
20	0.584
21	0.551
22	0.549
23	0.557
24	0.514
25	0.511
26	0.485
27	0.471
28	0.470
29	0.471
30	0.468

significant decrease in PWB heating rate is observed. Nonetheless, a higher fan frequency is always better than a lower one for heater protection purposes. Figure 3.10 shows temperature versus time curves for each of the 12 thermocouple locations during a convective heating experiment at a fan frequency of 23 Hz. Figure 3.10 as well as Table 3.2 shows that the PWB temperature rate is significantly lower than the desired temperature rate of 2 ^{o}C/second specified earlier. Figure 3.10 also illustrates that there is a slight variation in temperature across the PWB sample surface.

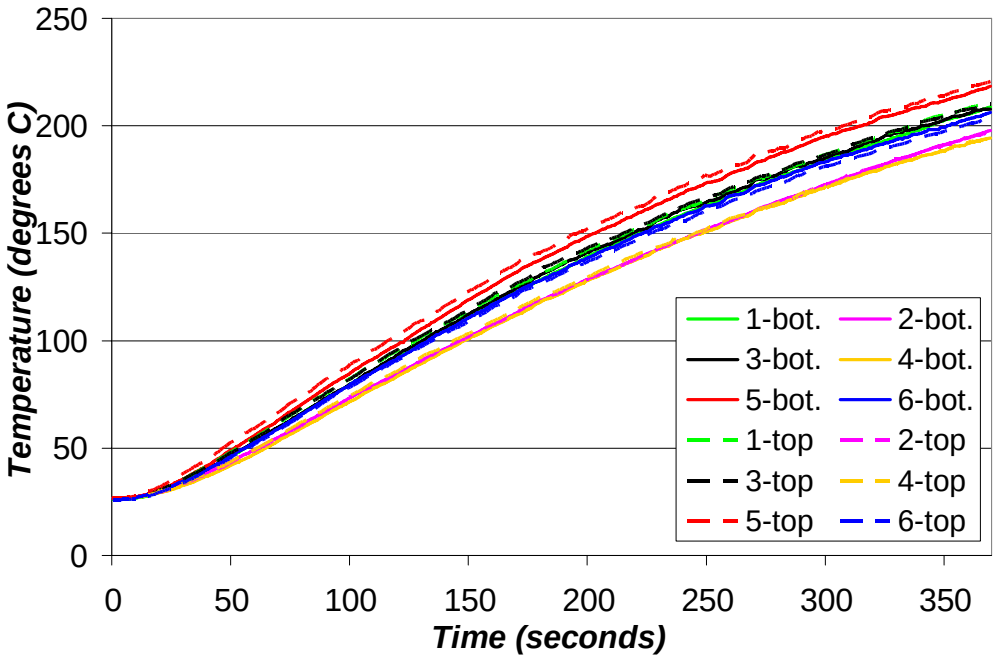


Figure 3.10. Thermocouple readings on a 203.2 mm by 139.7 mm by 0.631 mm PWB during convective heating

Table 3.3 shows the PWB through-the-thickness temperature difference at each of the 6 locations on the PWB shown in Figure 3.2. The highest PWB through-the-thickness temperature difference occurred at location 5 and was 4.8 ^{o}C. The lowest PWB through-the-thickness temperature difference occurred at location 2 and was 0.9 ^{o}C. A minus sign

Table 3.3. Maximum PWB through-the-thickness temperature difference during convective heating

PWB Thermocouple Locations	1	2	3	4	5	6
Maximum PWB Through-The-Thickness Temperature Difference during Convective Heating (^{o}C)	-3.5	-0.9	-3.2	-3.2	-4.8	3.1

in front of the PWB through-thickness temperature differences in Table 3.3 signifies that the PWB top surface is at a higher temperature than the PWB bottom surface. The PWB through-the-thickness temperature differences in Table 3.3 are significantly lower than the temperature differences in Table 3.1, which is expected since convective heating inherently heats more uniformly than infrared heating. The maximum through-the-thickness temperature difference of 41.6 ^{o}C obtained for infrared heating in Table 3.1 is 867 % higher than the maximum through-the-thickness temperature difference of 4.8 ^{o}C obtained for convective heating in Table 3.3. This shows that the convective system is significantly better than infrared heating with regards to PWB through-the-thickness temperature difference. In addition to the temperature difference through-the-thickness of the PWB, there is also some temperature variation on both the top and bottom sides of the PWB. On the PWB top side, the maximum temperature difference was 20.6 ^{o}C and occurred between thermocouple locations 2 and 5. On the PWB bottom side, the maximum temperature difference was 23.6 ^{o}C and also occurred between thermocouple locations 2 and 5. PWB/PWBA surface temperature variation also occurs in standard industrial reflow ovens. When the PWB sample shown in Table 3.2 was passed through an industrial seven chamber, forced convective reflow oven, the maximum observed surface temperature variation was 9 ^{o}C.

The developed convective reflow system was used to simulate a Lee optimized profile. The Lee profile was input to the oven's PID controller via the LABVIEW virtual instrument interface. Figure 3.11 shows the input and measured Lee optimized reflow profile used to reflow the PWBA. The feedback thermocouple used to measure the actual PWB temperature in-situ was placed directly at the center of the PWB's lower side.

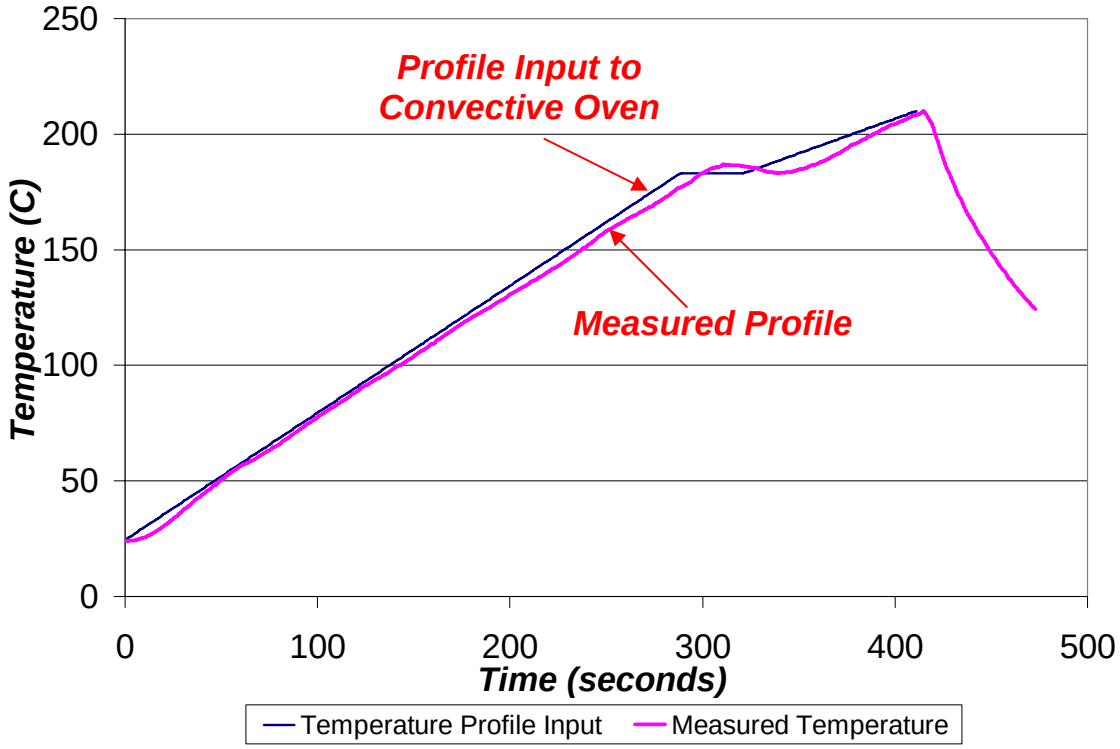


Figure 3.11. Simulation of Lee optimized reflow profile using the developed convective reflow system

The convective reflow profile shown in Figure 3.11 above has a ramp to dwell rate of 0.55 ^{o}C/second, a peak temperature of 208 ^{o}C and a time above liquidus of 79 seconds which is within the process window for the optimized Lee profile [70]. As Table 3.2 and Figure 3.10 above show, the PWB heating rate that the convective heating system can achieve should be improved in order to enable the system to simulate RDRP profiles. A computational fluid dynamics (CFD) model of the convective heating system was created in order to understand the critical system parameters and to determine methods to improve the system's heating performance.

CHAPTER 4

COMPUTATIONAL FLUID DYNAMICS MODEL OF CONVECTIVE REFLOW SYSTEM

As mentioned at the end of Chapter 3, a computational fluid dynamics model of the convective heating system was created in order to determine ways to improve its heating performance. A CFD model is versatile and allows virtual changes to be made to the system without having to spend thousands of dollars on the convective system in a trial and error approach. The CFD model can be used to perform design of simulation (DOS) analyses and subsequently, regression can be used to predict PWB heating rate with respect to system parameters.

4.1 Geometry Modeling

A three-dimensional (3D) model based on the geometry shown in Figure 3.8 was used for the CFD model. To simplify the geometry, all of the system ductwork was modeled such that a half-symmetry model could be created. However, the model geometry was created such that the model had the same volume of air as the real convective heating system as well as the same number and type of flow bends. The main geometrical components of the model were the 203.2 mm by 139.7 mm by 0.631 mm PWB, the 12 tubular heaters with 9.525 mm diameter, the oven chamber and the supporting ductwork. In the CFD analysis software, a fan is represented by a plane, so it

was unnecessary to model the complicated fan geometry. The meshed geometry will be shown in Section 4.3.

4.2 Material Properties

Several materials are used in the convective heating system. The PWB is a composite made up of copper and FR4, the oven chamber walls are made of stainless steel, the ductwork is made of carbon steel, and the heaters are made of a nickel-chromium alloy also known as Incoloy. Table 4.1 shows the thermal material properties used in the CFD model, which were obtained from literature [71, 72]. Note that Table 4.1 only shows room temperature thermal properties. However, temperature dependent thermal properties were used for air, carbon steel and stainless steel. The temperature dependent properties for air, carbon steel and stainless steel are included in Appendix A.1. For all other materials, room temperature properties were used which is sufficient for the CFD model.

Table 4.1. Room temperature thermal material properties used in CFD model

Material	Density (kg/m3)	Specific Heat (J/kg K)	Thermal Conductivity (W/m K)
Air	1.225	1006.43	0.0242
Carbon Steel	7854	434	60.1
Copper/FR4	2236	1113	22.5
Glass	2500	750	1.4
Incoloy	7940	460	11.5
Stainless Steel	7900	477	14.9

4.3 Meshing

The meshed convective heating system geometry is shown in Figure 4.1. The PWB in the CFD model was meshed using rectangular 3D elements. The air volume was meshed using tetrahedral elements to enable easy mapping of elements from the small PWB size to the large size of the oven chamber and surrounding ductwork. In the CFD analysis software, whenever a volume is meshed, all the associated faces in the model are also meshed automatically.

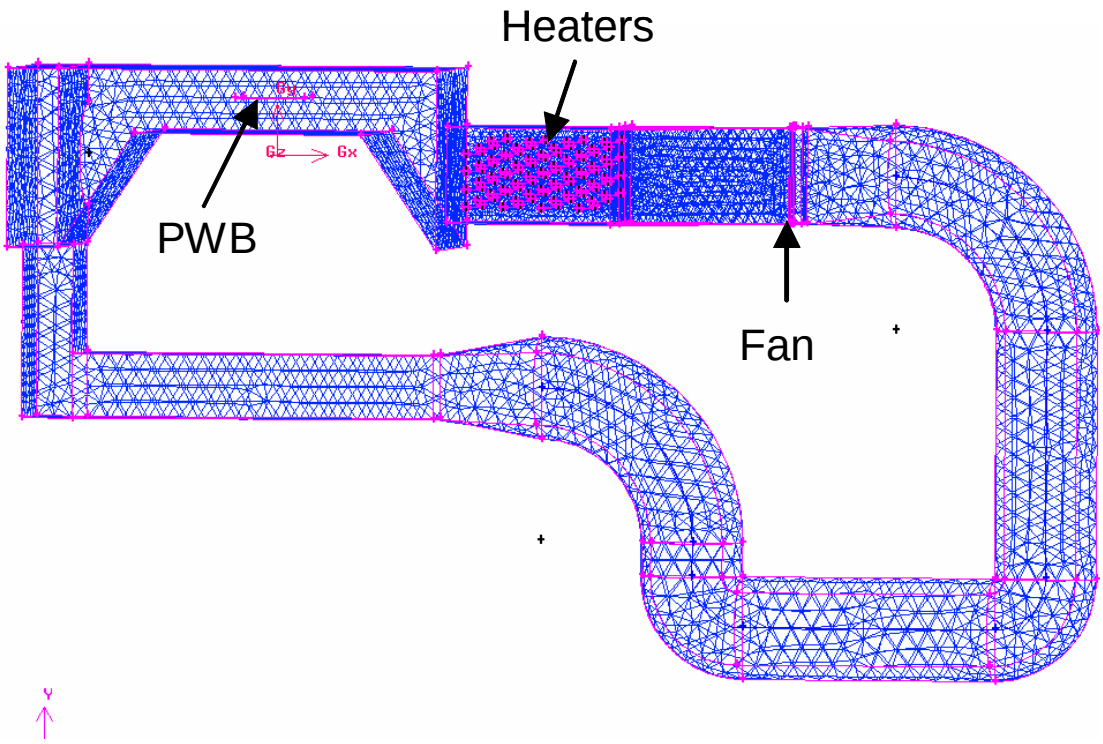


Figure 4.1. Meshed geometry of convective heating system

4.4 Boundary Conditions

The boundary condition for the tubular heaters was set by specifying the surface heat flux (62,000 W/m^2) of the heater walls. The heater surface flux is specified by the heater manufacturer. In the model, all the oven chamber and duct walls are assumed to be perfectly insulated. The boundary condition of the fan was set such that the fan outlet air velocity was 9.11 m/second which corresponds to a 23 Hz fan frequency discussed earlier. The fan outlet air velocity is kept constant for all of the cases discussed in this paper. In FLUENT, the only way to set the air velocity of the fan is to set the pressure across the fan boundary condition. In order to relate the pressure across the fan to air velocity, the fan performance curve is used. The fan performance curve is provided by the fan manufacturer and is shown in Figure 4.2.

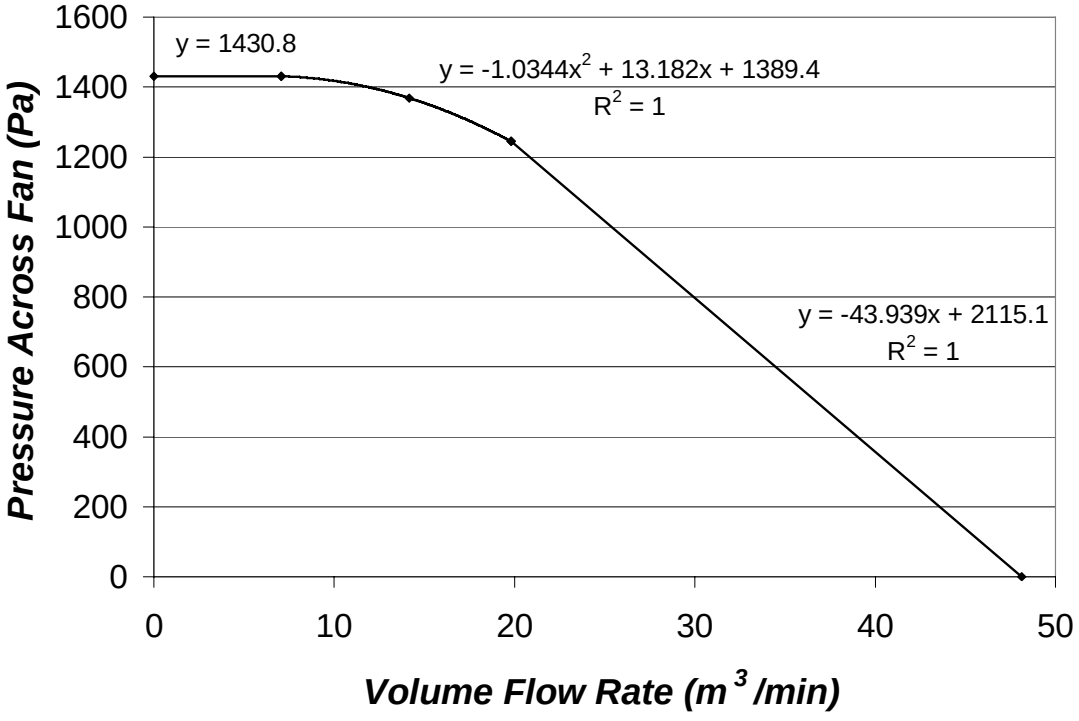


Figure 4.2. Fan performance curve

The fan used in the convective system operates at 35.40 m^3/min with a pressure drop of 622.1 Pa and 2745 RPM. As mentioned earlier, 23 Hz was chosen as the optimal fan frequency which corresponds to a fan outlet air velocity of 9.11 m/s. Since, the outlet area of the fan is 0.1778 m by 0.1397 m, an air velocity of 9.11 m/s corresponds to a volumetric flow rate of 13.57 m^3/min. In order to obtain the pressure across the fan for a flow rate of 13.57 m^3/min, the fan law equations shown in Equations 4.1 and 4.2 below must be used.

$$VFR_2 = \frac{FS_2}{FS_1} * VFR_1 \tag{4.1}$$

where,

FS = fan speed (RPM)

VFR = volumetric flow rate (m^3/min)

$$P_2 = \left(\frac{FS_2}{FS_1} \right)^2 * P_1 \tag{4.2}$$

where,

FS = fan speed (RPM)

P = pressure across fan (Pa)

Using Equation (4.1),

$$FS_2 = \left(\frac{13.57 m^3 / \min}{35.40 m^3 / \min} \right) * 2745\ rpm\ =\ 1053\ rpm$$

Using Equation (4.2),

$$P_2 = \left(\frac{1053\ rpm}{2745\ rpm} \right)^2 * 622.1\ Pa = 91.5\ Pa$$

Therefore, a fan outlet air velocity of 9.11 m/s corresponds to a pressure of 91.5 Pa across the fan. In order to model the fan correctly in FLUENT, the fan curve is input into the software as well as the desired air velocity of 9.11 m/s or the desired pressure across the fan of 91.5 Pa.

4.5 CFD Model Results

The temperature distribution of the PWB was extracted at 1 second time steps using a user defined subroutine written in C. The PWB temperature data along with time is then used to calculate PWB heating rate. Figure 4.3 shows a plot of average PWB

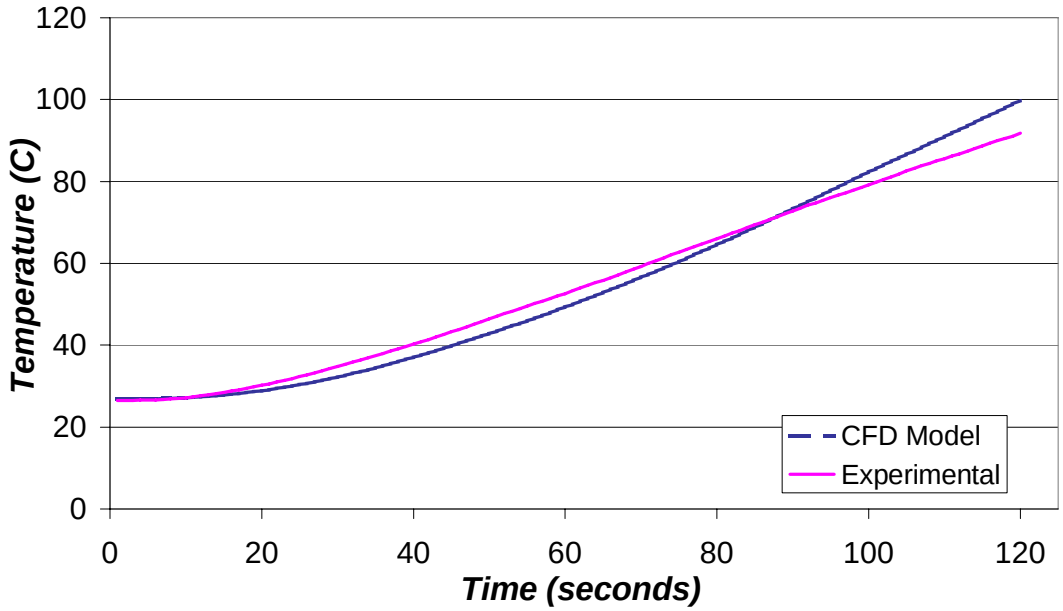


Figure 4.3. Comparison between CFD model and experimental results

temperature for experimental and CFD model results versus time during convective heating of a 203.2 mm by 139.7 mm by 0.631 mm PWB. For the CFD model, all nodal temperature values at each 1 second time step were averaged to obtain the curve in Figure 4.3. The CFD model was used to compute 120 time steps for a total time of 120 seconds. The purpose of the CFD model is to compute the PWB ramp rate that the convective heating system can achieve. In a typical reflow profile as shown in Figure 3.4, the maximum PWB/PWBA heating rate occurs in the ramp to dwell portion. To capture this PWB/PWBA heating rate, a total time of 120 seconds is sufficient.

A mesh convergence study was performed on the CFD model by reducing the size of all elements in the model by 25 %. Table 4.2 below shows a comparison between the PWB temperatures and PWB heating rates obtained from the original and reduced meshes. The percent difference between the PWB temperature obtained from the original mesh and the PWB temperature obtained from the reduced mesh was 2.6 %. The percent difference between the PWB heating rate calculated from the original mesh and the PWB heating rate calculated from the reduced mesh was 3.2 %. The percent difference results show that the mesh is converged.

Table 4.2. Mesh convergence results

	PWB Temperature at 120 seconds (^{o}C)	PWB Heating Rate (^{o}C/second)
Original Mesh	99.80	0.62
Reduced Mesh	97.23	0.60
Difference	2.6 %	3.2 %

For the experimental case, at each 1 second time step, the 12 thermocouple readings in Figure 3.10 were averaged to obtain the curve shown in Figure 4.3. Figure 4.3 shows that the CFD model agrees very well with experimental results between 0 and 120 seconds. Table 4.3 below shows a comparison between the PWB heating rate calculated using the CFD model and the PWB heating rate calculated using experimental data.

Table 4.3. Comparison between CFD model and experimental results

	PWB Temperature at 120 seconds (^{o}C)	PWB Heating Rate (^{o}C/second)
CFD Model	99.80	0.62
Experimental	91.84	0.56
Difference	8.8 %	10.7 %

The percent difference between the PWB temperature obtained from the CFD model and the PWB temperature obtained from experimental results was 8.8 %. The percent difference between the PWB heating rate calculated from the CFD model and the PWB heating rate calculated from experimental results was 10.7 %. These results as well as Figure 4.3 show that the CFD model agrees well with experiments. At time steps above 120 seconds, the CFD model tended to predict temperatures significantly higher than those obtained by experiments. This is expected, since the all ductwork and most oven walls in the model were assumed to be perfectly insulated, which is not the case in reality. The validated CFD model will now be used to perform a DOS and regression to aid in convective heating system improvement.

4.6 Design of Simulations and Regression

In order to determine how to improve the convective heating system, and to understand how convective heating system parameters affect PWB heating rate, a 3-factor, 2 level, full factorial DOS was performed using the CFD model. The factors of interest are convective heating system volume, surface area of the tubular heaters and power output of the heaters. The three factors of system volume, heater surface area, and heater power output will be varied in the model. Table 4.4 shows the simulation planning matrix as well as the PWB temperature after 120 seconds obtained from the CFD model for each run. The PWB temperatures obtained from the 8 runs of the DOS can be used to perform a regression analysis. In the regression equation, the response will be the PWB temperature at 120 seconds and the predictor variables are system volume, heater surface area and heater power.

Table 4.4. DOS planning matrix and PWB temperature results.

Run	System Volume (m^3)	Heater Surface Area (m^2)	Heater Power (kW)	PWB Temp. at 120 seconds (^oC)
1	0.32	0.58	36	102.60
2	0.39	0.58	36	99.80
3	0.32	2.32	36	185.57
4	0.39	2.32	36	174.41
5	0.32	0.58	72	177.45
6	0.39	0.58	72	173.87
7	0.32	2.32	72	345.20
8	0.39	2.32	72	327.12

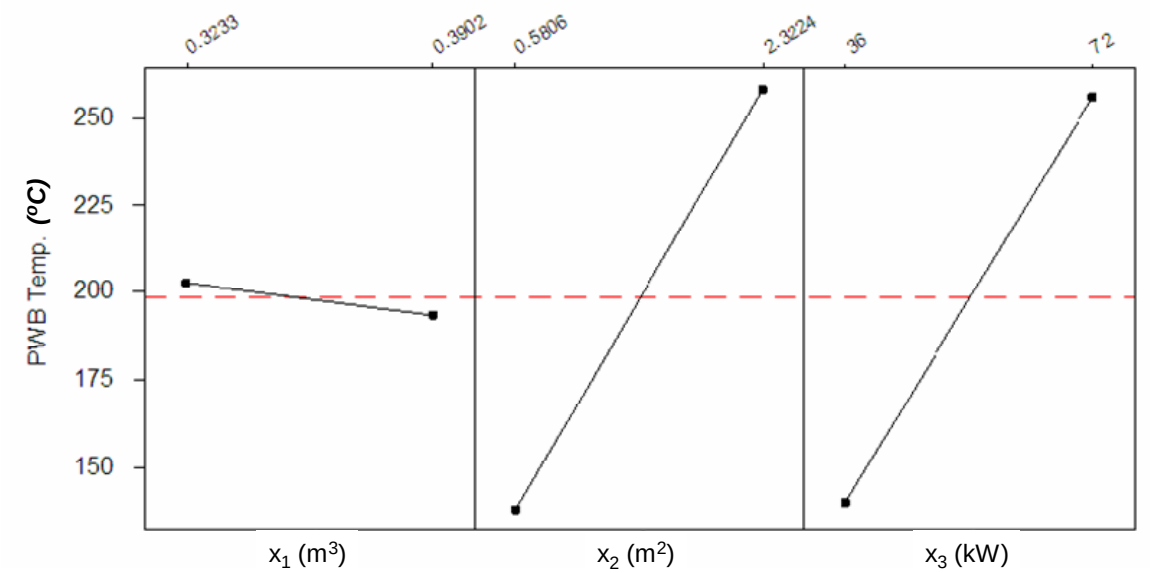


Figure 4.4. Main effects plots for DOS parameters. x_1 = system volume, x_2 = heater surface area, x_3 = heater power

Figure 4.4 shows the DOS main effects plot for the factors studied. For each factor, the main effect plot is simply constructed. For example, factor x_1 has two levels, 0.3233 m^3 and 0.3902 m^3. For each level, the temperature shown on the y-axis is calculated by averaging all the temperatures at that level in Table 4.4. For the 0.3233 m^3 level, the temperature plotted is the average of the temperatures from Run 1, Run 3, Run 5 and Run 7 in Table 4.4. Figure 4.4 shows that all three factors are significant with heater surface area and heater power being more significant than system volume.

In order to determine how to set the oven factors to obtain desired PWB heating rates, a regression was performed on the DOS results shown in Figure 4.4. PWB heating rates are easily calculated by taking the temperatures in Figure 4.4, subtracting 25 ^{o}C and then dividing the result by 120 seconds. Equation (4.3) shows a bilinear model expressing the response as a function of the predictor variables and their two-factor interactions.

$$Y = \beta_0 + \beta_1 x_1 + \beta_2 x_2 + \beta_3 x_3 + \beta_4 x_1 x_2 + \beta_5 x_1 x_3 + \beta_6 x_2 x_3 \qquad (4.3)$$

where,

Y = PWB temperature at 120 seconds (^oC)

x_1 = system volume (m^3)

x_2 = heater surface area (m^2)

x_3 = heater power (kW)

β_i = regression constants (i=0,1,2,3,4,5,6)

Note that the three-factor interaction, $x_1x_2x_3$, is omitted from Equation (4.3). $x_1x_2x_3$ is not included due to the hierarchical ordering principle which states that lower order effects are more likely to be important than higher order effects [73]. Also, if $x_1x_2x_3$ was left in the regression model, there would not be enough degrees of freedom to estimate the regression error. The regression constants β_i are calculated using Equation (4.4) which is the least squares estimate.

$$\hat{\beta} = \left(X^T X\right)^{-1} X^T y \tag{4.4}$$

where,

X represents the model matrix, and for this problem:

$$X = \begin{pmatrix} 1 & x_{1,1} & x_{2,1} & x_{3,1} & x_{1,1}x_{2,1} & x_{1,1}x_{3,1} & x_{2,1}x_{3,1} \\ 1 & x_{1,2} & x_{2,2} & x_{3,2} & x_{1,2}x_{2,2} & x_{1,2}x_{3,2} & x_{2,2}x_{3,2} \\ 1 & x_{1,3} & x_{2,3} & x_{3,3} & x_{1,3}x_{2,3} & x_{1,3}x_{3,3} & x_{2,3}x_{3,3} \\ 1 & x_{1,4} & x_{2,4} & x_{3,4} & x_{1,4}x_{2,4} & x_{1,4}x_{3,4} & x_{2,4}x_{3,4} \\ 1 & x_{1,5} & x_{2,5} & x_{3,5} & x_{1,5}x_{2,5} & x_{1,5}x_{3,5} & x_{2,5}x_{3,5} \\ 1 & x_{1,6} & x_{2,6} & x_{3,6} & x_{1,6}x_{2,6} & x_{1,6}x_{3,6} & x_{2,6}x_{3,6} \\ 1 & x_{1,7} & x_{2,7} & x_{3,7} & x_{1,7}x_{2,7} & x_{1,7}x_{3,7} & x_{2,7}x_{3,7} \\ 1 & x_{1,8} & x_{2,8} & x_{3,8} & x_{1,8}x_{2,8} & x_{1,8}x_{3,8} & x_{2,8}x_{3,8} \end{pmatrix}$$

T = matrix notation for transpose

y = Fifth column of Table 4.4 (PWB temperature at 120 seconds)

In regression analysis, most of the time, not all predictor factors are significant. Using the principle of parsimony, a model with a reduced number of predictors should always be used as long as it can represent the data well [73]. To generate the reduced model, a best subset regression is performed. In a best subset regression analysis, a model selection criterion is used to evaluate all possible sets of the predictors, and the reduced model with the best value of the criterion is chosen. Table 4.5 shows the result of the best subset regression.

Table 4.5. Best subset regression

Vars	R^2	R^2(adj.)	C_p	$MSE^{1/2}$	x_1	x_2	x_3	x_1 x_2	x_1 x_3	x_2 x_3
1	93.3	92.2	886.1	25.6						X
1	48.7	40.1	6803.6	70.9		X				
2	99.6	99.4	51.6	6.9			X			X
2	98.2	97.5	238.1	14.6					X	X
3	99.9	99.8	16.8	4.3			X		X	X
3	99.9	99.8	18.2	4.5	X		X			X
4	100.0	100.0	4.8	2.0		X	X	X		X
4	99.9	99.8	15.5	4.5			X	X	X	X
5	100.0	99.9	6.6	2.4		X	X	X	X	X
5	100.0	99.9	6.7	2.5	X	X	X	X		X
6	100.0	99.9	7.0	2.1	X	X	X	X	X	X

The model selection criterion that is used in this research is the Mallows' C_p statistic. The C_p statistic is defined using Equation (4.5).

$$C_p = \frac{RSS}{s_2} - (N - 2p) \tag{4.5}$$

where,

RSS = residual sum of squares for the model

s^2 = mean squared error for the model containing all covariates and a intercept term

N = total number of observations

If the model chosen is true,

$$E(RSS) = (N - P)\sigma^2$$

Assuming that $E(s^2) = \sigma^2$,

$$E(C_p) \approx \frac{(N-p)\sigma^2}{\sigma^2} - (N - 2p) = p$$

When the C_p statistic is used, the best model has a C_p that is close to the number of predictor variables + 1. Also, a secondary condition that should be met is that the best model should have the lowest C_p. As Table 4.5 shows, the best reduced model has a C_p of 4.8 and consists of the predictor x_2 (heater surface area), x_3 (heater power), x_1x_2 (interaction between system volume and heater surface area), and x_2x_3 (interaction between heater surface area and heater power. Equation (4.6) shows the regression equation of the best reduced model.

$$Y = 27.9 + 31.5\ x_2 + 1.31\ x_3 - 93.3\ x_1x_2 + 1.30\ x_2x_3 \tag{4.6}$$

To verify that Equation (4.6) is valid, a residual plot as well as a normal probability plot was created for the reduced model. The residual and normal probability plots are shown

in Figure 4.5 and Figure 4.6 respectively. The residual plot in Figure 4.5 is simply a plot of the error residuals for each run in the DOS. For each run, the error residual is the difference between the response Y value in Table 4.4 and the response value calculated using Equation (4.6). The normal probability plot in Figure 4.6 is slightly more complicated to generate. If the assumption is made that the residuals are normally distributed with the same variance, then $\Phi(\text{residual}_i)$ has a uniform distribution over [0,1].

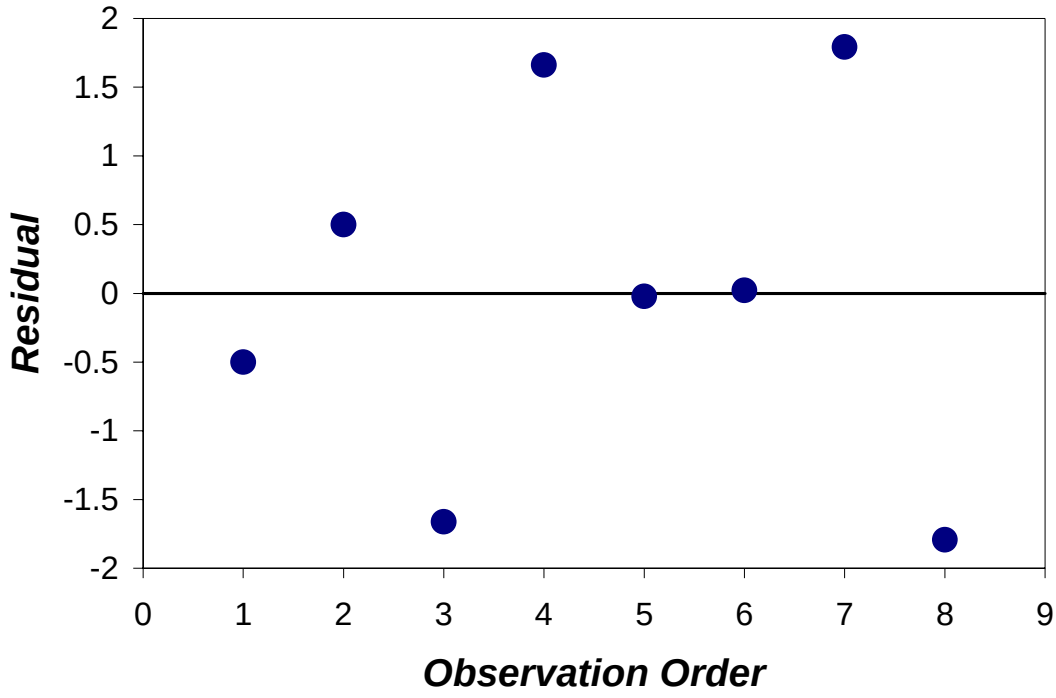


Figure 4.5. Residuals versus the order of the data for the reduced model.

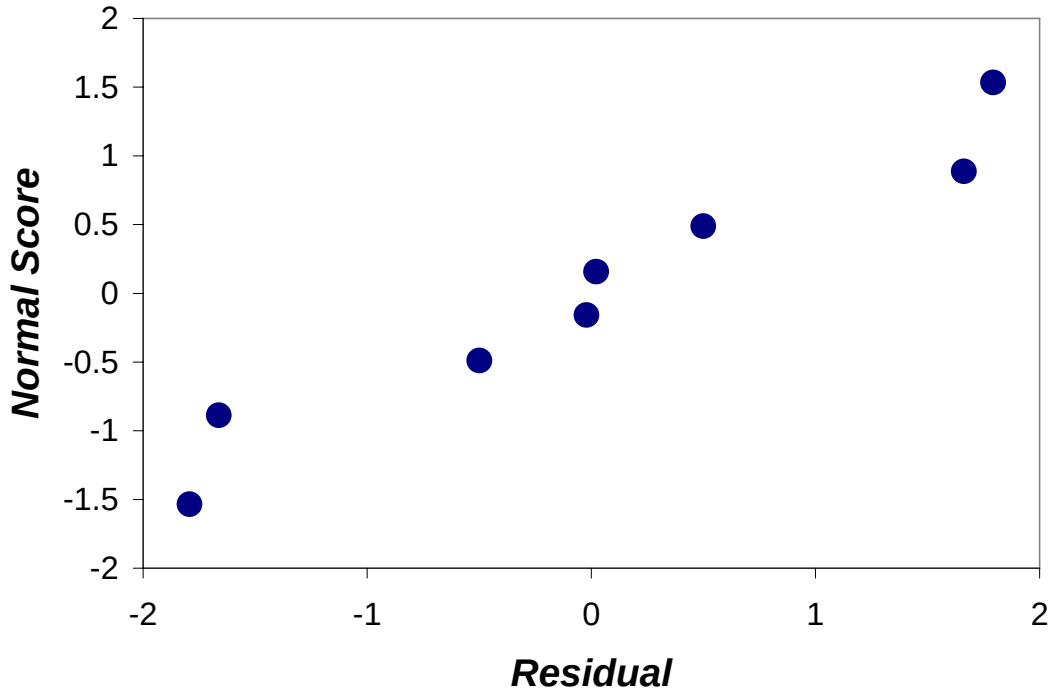


Figure 4.6. Normal probability plot of the residuals for reduced model.

This implies that the expected values of $\Phi(\text{residual}_i)$, i – 1,…, N are spaced uniformly over [0,1]. Therefore, the N points $(p_i, \Phi(\text{residual}_{(i)}))$ should lie on a straight line, where $p_i = (i - 0.5)/N$ [73]. The value used for i is the rank of the residual, therefore, the smallest residual will have an i value of 1. In the normal probability plot, the horizontal axis values are $\Phi^{-1}(p_i)$ where Φ^{-1} is the inverse normal distribution transformation. The vertical axis values in the normal probability plot are the residuals at each i value. Since the distribution of residuals in Figure 4.5 appears to be random, and the normal probability plot follows a linear trend, the model assumptions are correct and Equation (4.6) holds. To validate the regression model, another experimental test case was performed. The parameters chosen to test the regression model was a system volume of 0.39 m^3, a heater surface area of 0.58 m^2 and a heater power of 21.6 kW. These values

were input into the regression equation. The resulting PWB temperature at 120 seconds was:

$$Y = 27.9+31.5(0.58)+1.31(21.6)–93.3(0.39)(0.58)+1.30(0.58)(21.6) = 69.64\ ^{o}C$$

The corresponding PWB heating rate is:

$$\frac{69.64\ ^{o}C - 25\ ^{o}C}{120\,s} = 0.372\ ^{o}C/\mathrm{sec}ond$$

The PWB temperature at 120 seconds obtained from convective heating experiments using the above parameters was 76.01 ^{o}C. Note that a heater power of 21.6 kW was achieved experimentally by limiting the power supplied to the tubular heaters, which was done using a temperature controller. Therefore, the PWB heating rate obtained experimentally is:

$$\frac{76.01\ ^{o}C - 25\ ^{o}C}{120\,s} = 0.425\ ^{o}C/\mathrm{sec}ond$$

This represents a difference of 12.5 % showing that the regression equation is still valid for other parameter settings. Equation (4.6) can now be used to determine how to improve the convective heating system. Note that each of the original predictor variables of system volume, heater surface area and heater power are included in the regression equation. In order to achieve a 2 ^{o}C/second PWB heating rate to simulate RDRP convective reflow profiles, the PWB temperature after 120 seconds should be 265 ^{o}C. The current convective system configuration corresponds to Run 2 in Table 4.4. If all factors except system volume are kept constant, from Equation (4.6), the system volume necessary to produce a PWB heating rate of 2 ^{o}C/second is -2.67 m^3 which is clearly infeasible. If all factors except heater surface area are kept constant, from Equation (4.6), the heater surface area necessary to produce a PWB heating rate of 2 ^{o}C/second is 4.53

m^2. Note that increasing the surface area of a tubular heater would correspond to adding fins to the heater. If all factors except heater power are kept constant, from Equation (4.6), the heater power necessary to produce a PWB heating rate of 2 ^oC/second is 116.20 kW. The three cases presented above provide meaningful information. First, for the system volume case, creating a design with a negative volume is impossible. For the heater surface area case, a heater surface area of 4.53 m^2 represents a surface area increase of 8 times over the original tubular heaters. No tubular heater with fins is available that provides a surface area increase of 8 times over an unfinned heater. For the heater power case, tubular heaters that would output a total of 116.20 kW over such a small heater surface area don't exist. Therefore, the above three cases show that all factors must be changed simultaneously in order to achieve the desired PWB ramp rate.

Table 4.6 shows possible oven parameter settings that would result in PWB heating rates of 1 ^oC/second, 1.5 ^oC/second, 2 ^oC/second and 2.5 ^oC/second respectively.

Table 4.6. Possible oven parameter settings to achieve desired PWB heating rates

Desired PWB Heating Rate (^oC/second)	System Volume (m^3)	Heater Surface Area (m^2)	Heater Power (kW)
1.0	0.39	1.67	36
1.5	0.35	2.32	42
2.0	0.33	2.32	54
2.5	0.32	2.32	68

CHAPTER 5

DEVELOPMENT OF A PROJECTION MOIRÉ MEASUREMENT SYSTEM

The projection moiré optical setup and measurement process was described earlier in Chapter 2. In this chapter, an automatic chip package detection algorithm is developed and implemented for use with the projection moiré warpage measurement system. The algorithm is designed to be a post-processing algorithm and is used after experiments are completed. The motivation and methodology of the algorithm are discussed below.

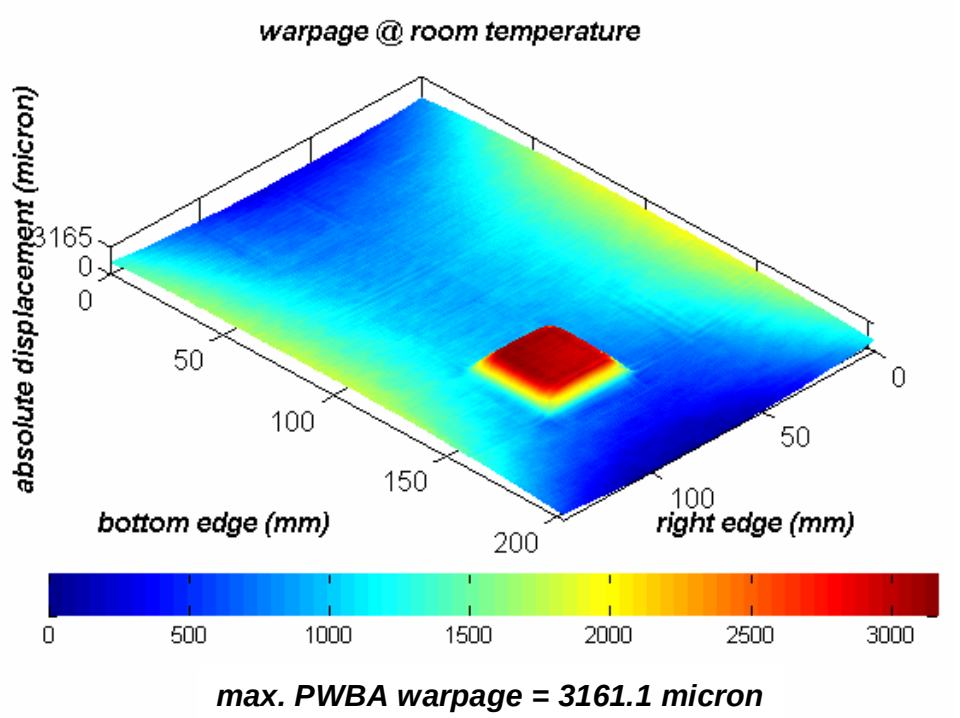


Figure 5.1. Projection moiré out-of-plane displacement plot of a PWB with loose PBGA package

5.1 Projection Moiré System Post-processing

Figure 5.1 shows an out-of-plane displacement plot of a PWB with one PBGA package obtained from the projection moiré measurement system. The PBGA package is a 35 mm peripheral array package with 352 solder bumps and a pitch of 1.27 mm. The quantitative maximum PWBA warpage result shown in Figure 5.1 of 3,161.1 microns is correct for PWBA warpage but incorrect if the warpage of the PWB only is of interest. For a bare PWB, maximum PWB warpage is calculated by taking the difference between the maximum PWB out-of-plane displacement and the minimum PWB out-of-plane displacement. However, for a PWB with chip packages, this calculation is incorrect if the maximum out-of-plane displacement is taken as a point on the tallest chip package as shown in Figure 5.1. Therefore, in order to calculate maximum PWB warpage correctly for a PWBA, the areas occupied by the chip package(s) should not be used in the calculation. From a visual estimation using Figure 5.1, the PWB warpage value should be close to 2,000 microns. In order for maximum PWB warpage for a PWBA to be calculated in an automatic fashion, an algorithm must be developed that can automatically segment the chip package locations from the rest of the PWB. In addition, the segmented chip package areas can be used to calculate the maximum warpage of the chip packages. The second objective of this research is to develop an automatic chip package detection algorithm for the projection moiré system. The automatic chip package segmentation algorithm is discussed next.

5.2 Automatic Chip Package Segmentation Algorithm

5.2.1 Image Segmentation Method Selection

Several segmentation methods were considered for the projection moiré system used in this research. The first method that was considered was a manual segmentation method. In this method, the gerber file for the PWBA is used to determine the locations of the chip packages. The chip packages can be masked by manually inputting the chip package locations and the chip package sizes from the gerber file into the warpage calculation software. The manual segmentation method may not be an accurate segmentation, and it would be tedious. For every PWBA sample to be tested, the gerber file would be needed. It would also be very time consuming to enter the chip package locations and sizes into the warpage calculation software after every measurement point. It should be noted that chip package coordinates obtained from the gerber file assumes that the PWB is perfectly flat. On warped PWBs, the chip package coordinates obtained from the gerber file will be inaccurate for the warped PWB. Due to the tedious nature of manual segmentation, automatic segmentation methods were explored. An automatic segmentation algorithm would not require the experimenter to know the exact chip package sizes or locations a priori or to perform tedious post-processing operations after experiments.

The simplest type of image segmentation that could be used for segmenting the chip packages is thresholding [74]. The thresholding technique involves setting a threshold in which the pixels in the image above the threshold are regarded as the segmented object, while the pixels below the threshold are regarded as background. For this warpage measurement application, the threshold would be an out-of-plane

displacement value. Figure 5.1 shows that the height of the PBGA package is much larger than the maximum out-of-plane displacement difference across the surface of the PWB. Therefore, in this case, the areas of the image in Figure 5.1 above the preset threshold would be regarded as chip package locations. Unfortunately, thresholding would not be a very robust method of segmenting the chip packages from the PWB. Any threshold that would segment the chip package in Figure 5.1 would also segment areas of the PWB. This is because the left edge of the PWB in Figure 5.1 is just as tall as the outer parts of the PBGA package. Thresholding would only work if the chip package and the PWB areas just outside the chip package had the largest surface displacements. Also, if thresholding was used for segmentation, the preset threshold would vary for each PWBA being tested. Since thresholding was ruled out as a way to segment chip packages from the PWB, edge based segmentation techniques were explored next.

Edge based segmentation techniques are based on the principle of finding the edges in the image of interest. The edges of an image, f, are found by taking the two-dimensional gradient given by Equation (5.1).

$$\nabla f = [G_x + G_y]^{\frac{1}{2}} \tag{5.1}$$

where,

∇f = image gradient

G_x = gradient for vertical edges

G_y = gradient for horizontal edges

For computational ease, Equation (5.1) is approximated by Equation (5.2) below.

$$\nabla f \approx \left|G_x\right| + \left|G_y\right| \tag{5.2}$$

The gradients G_x and G_y can be estimated in many ways such as using masks as shown in Figure 5.2. There are several gradient estimation masks available. The Sobel masks shown in Figure 5.2 below tend to be very popular. The values z_1 to z_9 in Figure 5.2

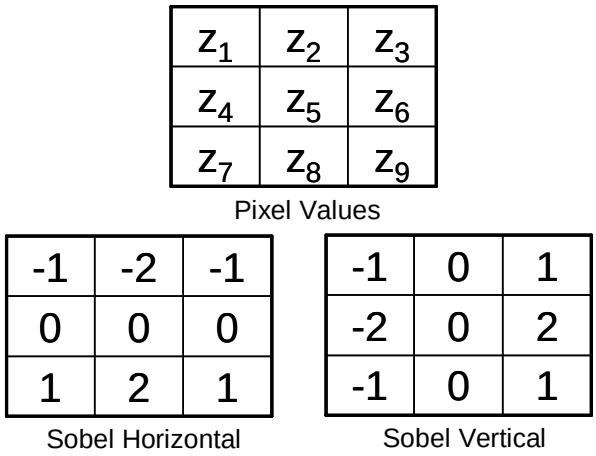


Figure 5.2. Sobel masks for image gradient estimation

represents a 3 x 3 section of the original image for which edges are sought. Figure 5.2 shows Sobel horizontal and vertical masks for calculating the values for each pixel in an edge image. The pixel value for z_5 in the edge image is calculated by multiplying each value in the mask by the corresponding value in the original image and summing the result. Therefore, using the Sobel horizontal and vertical masks would yield the following results for G_x and G_y for the edge image pixel corresponding to z_5 in the original image.

$$G_x = (z_3 + 2z_6 + z_9) - (z_1 + 2z_4 + z_7)$$

$$G_y = (z_7 + 2z_8 + z_9) - (z_1 + 2z_2 + z_3)$$

After the horizontal and vertical image gradients are computed, the edge direction, θ, can be determined using Equation (5.3).

$$\theta = inv\tan\left(\frac{G_y}{G_x}\right) \tag{5.3}$$

In an ideal world, implementing the Sobel edge detection masks on real life images would yield all the edges in the image perfectly. Unfortunately, due to noise and other issues, this is not always the case. To circumvent some of the problems with only using masks such as Sobel masks to find edges in real images, Canny developed an optimal edge detector [75]. In the Canny edge detection method, before determining the horizontal and vertical gradients using Sobel masks as shown in Figure 5.2, image noise is filtered out using a Gaussian filter. A Gaussian filter is used, because it can be computed using a simple mask. Once a suitable mask has been calculated, Gaussian smoothing can be performed using standard convolution methods. A convolution mask is usually much smaller than the actual image. As a result, the mask is slid over the image, manipulating a square of pixels at a time. The larger the width of the Gaussian mask, the lower is the detector's sensitivity to noise. The localization error in the detected edges also increases slightly as the Gaussian width is increased. The standard Gaussian function in 2D form is shown in Equation (5.4).

$$G(x,y) = \frac{1}{2\pi\sigma^2} e^{-\frac{x^2+y^2}{2\sigma^2}} \tag{5.4}$$

Figure 5.3 shows a discrete approximation to the Gaussian in the form of a mask as discussed earlier.

$$\frac{1}{331}\begin{bmatrix} 1 & 4 & 7 & 4 & 1 \\ 4 & 20 & 33 & 20 & 4 \\ 7 & 33 & 55 & 33 & 7 \\ 4 & 20 & 33 & 20 & 4 \\ 1 & 4 & 7 & 4 & 1 \end{bmatrix}$$

Figure 5.3. Discrete approximation to Gaussian function with $\sigma = 1$.

The mask in Figure 5.3 is approximated by two-dimensional sampling of the function shown in Equation (5.4). In the Canny edge detection technique, after the image is filtered using a Gaussian filter and the edges are found using Sobel masks, the next step is to implement a process called nonmaxima suppression. Nonmaxima suppression is used to trace along the edge in the edge direction and suppress any pixel value (by setting it equal to 0) that is not considered to be an edge. The final step in Canny edge detection is double thresholding which minimizes the breaking up of noisy edges into multiple edge segments. In double thresholding, two thresholds, T_1 and T_2, are used to determine if a pixel lies on an edge. Any pixel in the image that has a value greater than T_1 is presumed to be an edge pixel, and is marked as such immediately. Then, any pixels that are connected to this edge pixel and that have a value greater than T_2 are also selected as edge pixels. Figure 5.4 below shows the edge image corresponding to the surface displacement image in Figure 5.1 when the Canny edge detection method is used.

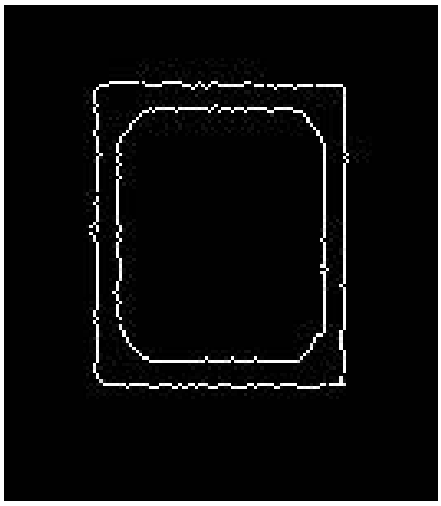


Figure 5.4. Canny edge detection of PBGA package

The PBGA package is clearly visible in the edge image shown in Figure 5.4. This is due to the fact that there are large changes in out-of-plane displacement at the PBGA edges. Therefore, the Canny edge detector can find the edges of the PBGA package. Once the edges of the chip package are found as shown in Figure 5.4, the location of the chip still remains unknown. The chip package can be readily identified by a person viewing the edge image, but the software is still unaware of the exact chip package location.

To determine the exact location of the chip package, a search algorithm must be implemented. A search technique that was considered for this problem of finding the exact chip package location was the object recognition algorithm developed by Steger [76]. Steger's technique involves several steps. The first step involves obtaining a test image with a shape similar to the one that will be tested. In this case, if the location of a PBGA package needs to be determined, a test image containing a PBGA package is used. The next step involves filtering the test image with a Gaussian filter and then extracting the edges of the image using an edge detector. After the edges are obtained, the entire image is searched to obtain the pixels that correspond to the chip package edges. For each

pixel that corresponds to an edge, the gradient direction is calculated. At this point, the characteristics of the test image are known. Steger's algorithm works on the principle that the image of interest will be searched for similarities with the test image. The image of interest such as Figure 5.1 is first filtered using a Gaussian filter and then the image edges are found using edge detectors such as the Canny edge detector. The pixels corresponding to the edges in the test image are then dotted with the entire image of interest, at all possible locations. The location that has the highest dot product corresponds to the chip package location. There are several drawbacks in using the Steger technique with the projection moiré warpage measurement system. The first problem is that a test image would need to be created for every type of chip package that would be measured using the system. Also, if the chip package used in the test image was exactly the same as the chip package in the image of interest, but the zoom of the camera was changed slightly between the time the test image was created and when the image of interest was analyzed, the algorithm may not find the chip package correctly. Due to the shortcomings of the Steger objection detection method for this projection moiré warpage measurement system, the method of active contours was used to determine the exact locations of chip packages. Active contours are explained in the next section.

5.2.2 Active Contour Models and Greedy Algorithm

In order to find the precise location of the chip package(s) in an out-of-plane displacement image, active contours were used. Active contours or snakes were developed by Kass et al. and are energy minimizing splines that are guided by external constraint forces and influenced by image forces that pull it toward features such as lines

and edges in an image [77]. Williams and Shah developed the Greedy algorithm which is a fast and stable numerical approach for solving the energy minimization problem [78]. The energy quantity being minimized by the Greedy algorithm is shown in Equation (5.5).

$$E = \int (\alpha(s)E_{cont} + \beta(s)E_{curv} + \gamma(s)E_{image})\, ds \tag{5.5}$$

where,

α, β, γ = weighting parameters

E_{cont} = continuity term

E_{curv} = curvature term

E_{image} = image gradient term

E_{cont} is the continuity term that ensures that the points on the contour are evenly spaced and that the curve remains smooth. E_{curv} is the curvature term. E_{curv} is calculated at each point on the contour, and if the curvature between the current point and adjacent points is above a certain value, the current point becomes a corner. E_{image} is the image force, which is gradient magnitude. Specifically, E_{image} is the negative of gradient magnitude, so that locations in the image with high gradient will minimize the energy, E, in Equation (5.5). α, β, γ are parameters used to weight the importance of each term in Equation (5.5). For the purpose of edge finding, γ should be set higher than α and β. An analysis of the effects of each weighting parameter on the converged snake will be discussed below.

When active contours are used for edge detection, an initial contour is constructed around the edges of interest. Figure 5.5 shows an example of an initial contour with 24 points constructed around the chip package of interest.

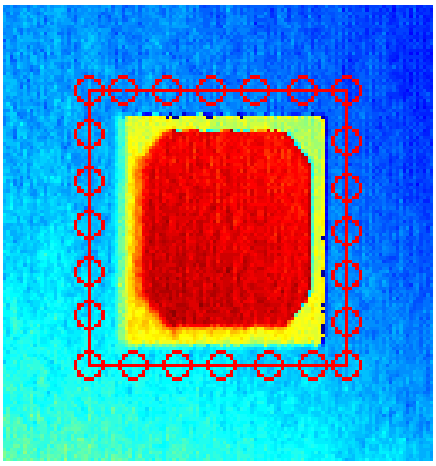


Figure 5.5. Initial contour around PBGA package

At each point on the snake, the energy from Equation (5.5) is computed. For each snake point, the energy is also calculated for the surrounding pixels. The neighborhood of pixels around each snake point is searched for the lowest energy point when compared to the energy of the current point. The current point is then moved to the lowest energy point. This process is repeated for all points on the contour until each point on the contour is a minimum energy point. The points of minimum energy in the image will correspond to edges in the image based on the formulation of Equation (5.5).

In order to characterize the Greedy algorithm for edge detection of chip packages, a test out-of-plane displacement image was created. The test image consisted of a flat surface and a square block with a certain height. The flat surface represents the PWB and the block represents an arbitrary chip package. The test image represents an ideal case and is used to verify that active contours with the Greedy algorithm are appropriate for the problem at hand. Figure 5.6 shows the test image.

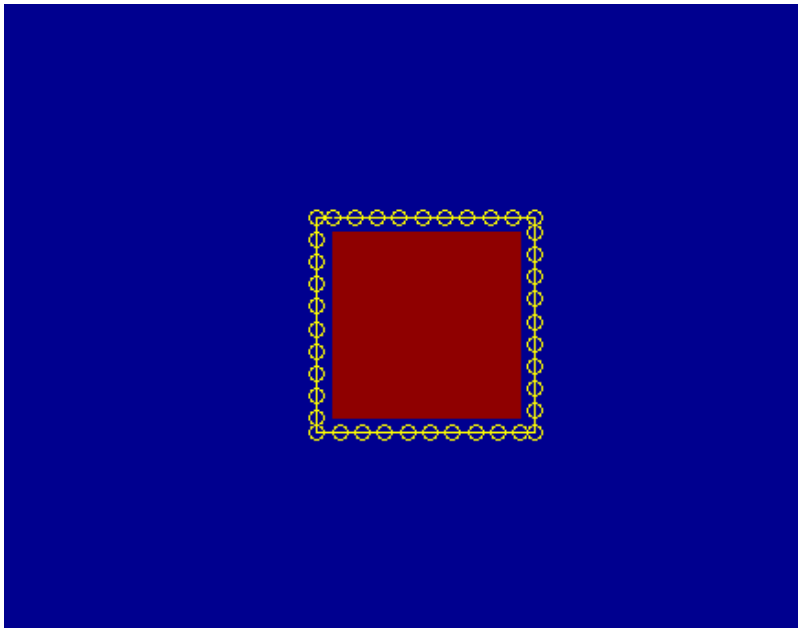


Figure 5.6. Test image used for Greedy algorithm characterization

The test image in Figure 5.6 was constructed to have 480 pixels in the y direction and 512 pixels in the column direction, which gives an image with similar dimensions as out-of-plane displacement images obtained from the projection moiré system. The test image was used to study the effects of algorithm variables on Greedy algorithm convergence. The variables studied were the weighting parameters, α, β, and γ, the size of the search neighborhood around each point on the snake. the number of points on the snake and the initial size of the snake relative to chip package size.

Figure 5.7 shows converged snakes for varying values of α, β, and γ. The only snake that converged onto the simulated chip package edge was the case where γ is

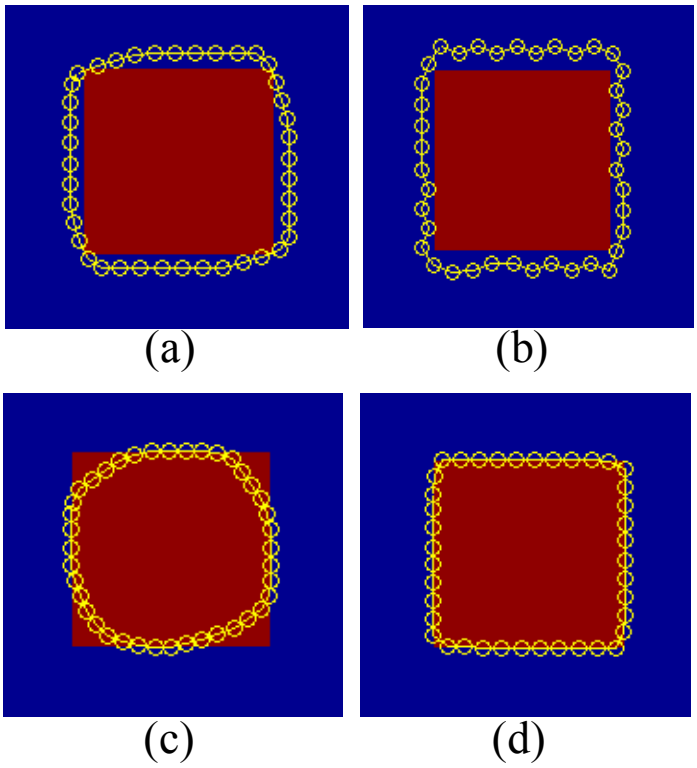


Figure 5.7. Converged snake for varying values of α, β and γ. (a) α, β, γ = 1. (b) α = 8, β, γ = 1. (c) α = 1, β = 8, γ = 1. (d) α, β = 1, γ = 8.

greater than α and β. This is expected, because γ is the weighting parameter associated with the image gradient and therefore should be the most influential parameter. As mentioned earlier, for each iteration of the Greedy algorithm, the neighborhood of each snake point is searched to determine the point's next location. Table 5.1 shows a comparison between the algorithm convergence times for varying neighborhood sizes. Note that the algorithm was run on a 2.8 GHz computer. The absolute convergence time

Table 5.1. Convergence time versus snake search neighborhood size

Neighborhood Size (pixels)	Convergence Time (seconds)
3 x 3	1.2190
5 x 5	0.5620
7 x 7	1.5630

is not as important as the relative times between the cases. Table 5.1 shows that the optimal neighborhood size is 5 pixels by 5 pixels, since it had the lowest convergence time of 0.5620 seconds which is 54 % shorter than the convergence time for a 3 pixel by 3 pixel neighborhood and 64 % shorter than the convergence time for a 7 pixel by 7 pixel neighborhood. For the 3 pixel by 3 pixel case, the small neighborhood is searched rapidly, but the small neighborhood causes more searches to be performed until snake convergence. For the 7 pixel by 7 pixel case, even though fewer neighborhood searches for convergence are performed, the search of each 7 pixel by 7 pixel neighborhood takes a significant amount of time. The 5 pixel by 5 pixel neighborhood is the optimal size between the two extremes.

Figure 5.8 shows a plot of algorithm convergence time versus the number of snake points. Figure 5.8 shows that snake convergence time increases only slightly with the number of snake points. For every point added to the snake, the convergence time increases by 0.84 %. Figure 5.9 shows a plot of snake convergence time versus the distance between the initial snake and the chip package edge. Note that as this distance increases, the initial snake increases in size. For every pixel added to the distance between the initial snake and chip package edge, the convergence time increases by 19

%. Therefore, the initial snake size should be as close as possible to the size of the chip package of interest to save computation time.

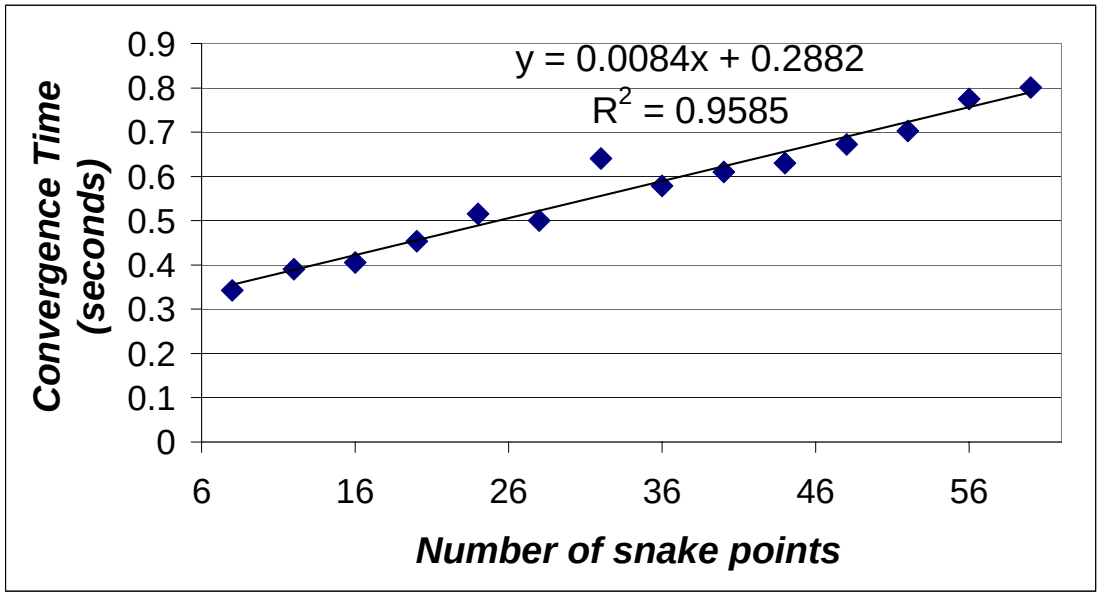


Figure 5.8. Algorithm convergence time versus number of points on snake

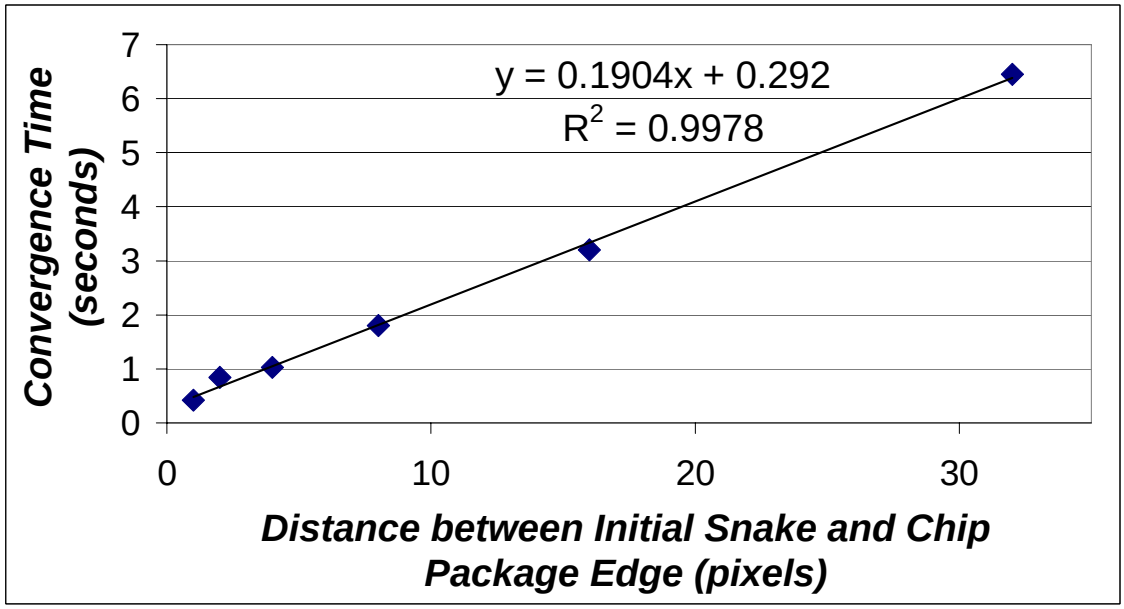


Figure 5.9. Algorithm convergence time versus distance between initial snake and chip package edge

5.2.3 Automatic Construction of Initial Snake

In order to use snakes and the Greedy algorithm to find the chip packages in the out-of-plane displacement image of a PWBA, the initial snake must be constructed. In this section, an algorithm that automatically contructs the initial snake is described. The first step in constructing the initial snake is to find the edge image using the Canny edge detector as shown in Figure 5.4 above. After finding the edge image, the 480 pixel by 512 pixel edge image is subsampled to obtain a 60 pixel by 64 pixel image. The image is subsampled to remove pixel discontinuities and because a subsampled image is much easier to search than a larger image. In this case, subsampling to a 60 pixel by 64 pixel image reduces the number of pixels by 64 times. Also, each pixel in the subsampled image represents 8 pixels in the original image. Therefore, after the initial snake is constructed, it will be between 1 and 8 pixels away from the chip package edge. The subsampled edge image can now be searched to find the general locations of the chip packages. Figure 5.10 shows an example of a matrix of pixel values of a subsampled edge image. In Figure 5.10, all nonzero values in the pixel matrix represent chip package edges. Note that Figure 5.10 only shows a small portion of the subsampled edge image. The subsampled edge image will be used to find the outline of the chip package so that the intial snake can be constructed for the Greedy algorithm. Figure 5.10 shows a typical scenario that the automatic snake construction algorithm must contend with. In Figure 5.10, two distinct edges can be seen on each side of the chip package, the edge corresponding to the BGA substrate and the edge corresponding to the molding. After the subsampled edge image is obtained, the entire image is searched for the pixel with the

0	0	0	0	0	0	0	0	0
0	**0.21**	**0.19**	**0.20**	**0.19**	**0.20**	**0.19**	**0.21**	0
0	**0.20**	0	**0.21**	**0.20**	**0.20**	0	**0.20**	0
0	**0.20**	**0.20**	0	0	0	**0.20**	**0.19**	0
0	**0.21**	**0.19**	0	0	0	**0.20**	**0.20**	0
0	**0.19**	**0.20**	0	0	0	**0.19**	**0.19**	0
0	**0.19**	0	**0.19**	**0.20**	**0.20**	0	**0.20**	0
0	**0.21**	**0.20**	**0.19**	**0.21**	**0.20**	**0.20**	**0.21**	0
0	0	0	0	0	0	0	0	0

Figure 5.10. A 9 by 9 pixel portion of the 60 by 64 pixel subsampled edge image matrix showing chip package location. Top left corner corresponds to pixel (30, 32).

maximum gradient. After the pixel with maximum gradient is found, the chip package outer bounds can be easily found. In Figure 5.10, the maximum gradient value is 0.21, and the maximum occurs at seven pixel locations which may be typical for a real PBGA. After the location of the pixel having the maximum gradient is found, the image is traversed from that pixel in both the horizontal and vertical directions giving a total of four paths from the pixel having maximum gradient. The algorithm will traverse each of the four paths until it encounters three zeros in a row. This condition is set such that if for any instance, the edge after subsampling is still noisy and has two gaps in the subsampled image, the algorithm will still work. After traversing each of the four paths until three zeros are found, the algorithm stores the location of the nonzero pixel in each direction just before the three zeros are encountered. At this point, since the horizontal and vertical directions have been traversed, the algorithm knows the maximum and minimum horizontal and vertical coordinates for one of the chip package edges. A conditional

statement is then executed. If the maximum horizontal coordinate minus the minimum horizontal coordinate is less than three, then the algorithm knows that a vertical edge has been detected. Therefore, the algorithm knows that the horizontal chip package edges in the subsampled image still need to be traversed. The horizontal edges are traversed by going to the pixel locations at the maximum and minimum vertical coordinates and traversing horizontally until three zeros in a row are encountered as discussed previously. At this point the maximum and minimum coordinates in both the horizontal and vertical directions are known and will bound the chip package of interest. Likewise, if after the very first direction traversal of the subsampled image, the maximum vertical coordinate minus the minimum vertical coordinate is less than three, then the algorithm knows that a horizontal edge has been detected. Therefore, the algorithm knows that the vertical chip package edges in the subsampled image still need to be traversed. The vertical edges are traversed by going to the pixel locations at the maximum and minimum horizontal coordinates and traversing vertically until three zeros in a row are encountered as discussed previously. At this point the maximum and minimum coordinates in both the horizontal and vertical directions are known and will bound the chip package of interest. For demonstration purposes, it can be assumed that the top left nonzero pixel in Figure 5.10 corresponds to pixel (30,32) where 30 is the vertical coordinate and 32 is the horizontal coordinate, where the origin is taken from the upper left corner of the image. From Figure 5.10, the pixel location having the maximum gradient at the center of the bottom edge is located at (36,35). Using the algorithm, starting from this pixel the image is traversed in both directions (four paths total) until three zeros are obtained. It can be assumed that only zeros occur outside the bounds of the subsampled image shown in

Figure 5.10. At this point, the minimum horizontal coordinate is 32 and the maximum horizontal coordinate is 38. The minimum vertical coordinate is 35 and the maximum vertical coordinate is 36. Since the range of vertical coordinates is less than three, the algorithm goes to the pixels located at (36,32) and (36,38) and then traverses the image along the vertical directions until three zeros are found along the available paths. At this point, the algorithm knows that the minimum horizontal coordinate is 32, the maximum horizontal coordinate is 38, the minimum vertical coordinate is 30 and the maximum vertical coordinate is 36.

After the lower and upper bound coordinates of the chip package are found in both directions for the subsampled image, the initial contour can be constructed after converting the coordinate bounds in the subsampled image to bounds in the original image. The lower and upper bound values of the chip package in the 60 by 64 pixel subsampled image is converted to upper and lower bound values of the chip package in the original edge image using Equations (5.6) to (5.9).

$$LBO_{horiz.} = (LBS_{horiz.} - 1) * (8) \tag{5.6}$$

$$LBO_{vert.} = (LBS_{vert.} - 1) * (8) \tag{5.7}$$

$$UBO_{horiz.} = (UBS_{horiz.}) * (8) \tag{5.8}$$

$$UBO_{vert.} = (UBS_{vert.}) * (8) \tag{5.9}$$

where,

LBO_i = lower bound in original image for direction i

LBS_i = lower bound in subsampled image for direction i

UBO_i = upper bound in original image for direction i

UBS_i = upper bound in subsampled image for direction i

After the lower and upper bound coordinate values in the original edge image are known, a rectangular snake with any number of points can be easily constructed around the location of the chip package. The Greedy algorithm can then be used to converge the initial snake onto the chip package edges. For PWBAs with multiple chip packages, the entire process described in this section is repeated for each chip package. However, after the lower and upper bound coordinate values for a chip package are found from the subsampled edge image, all pixel values corresponding to that chip package are zeroed out before searching the subsampled edge image for subsequent chip packages.

5.3 PWBA Warpage Measurements Using Automatic Chip Package Detection Algorithm

To test the automatic chip package detection algorithm described in the previous section, the projection moiré system was used to measure PWBs with PBGA packages. The PBGA packages tested were a 27 mm PBGA package with 256 solder bumps and a 35 mm PBGA package with 352 solder bumps. Both PBGA chip packages had a pitch of 1.27 mm. The PWB measured was 203.2 mm by 139.7 mm by 0.631 mm. Figure 5.11 and Figure 5.12 show out-of-plane displacement plots obtained

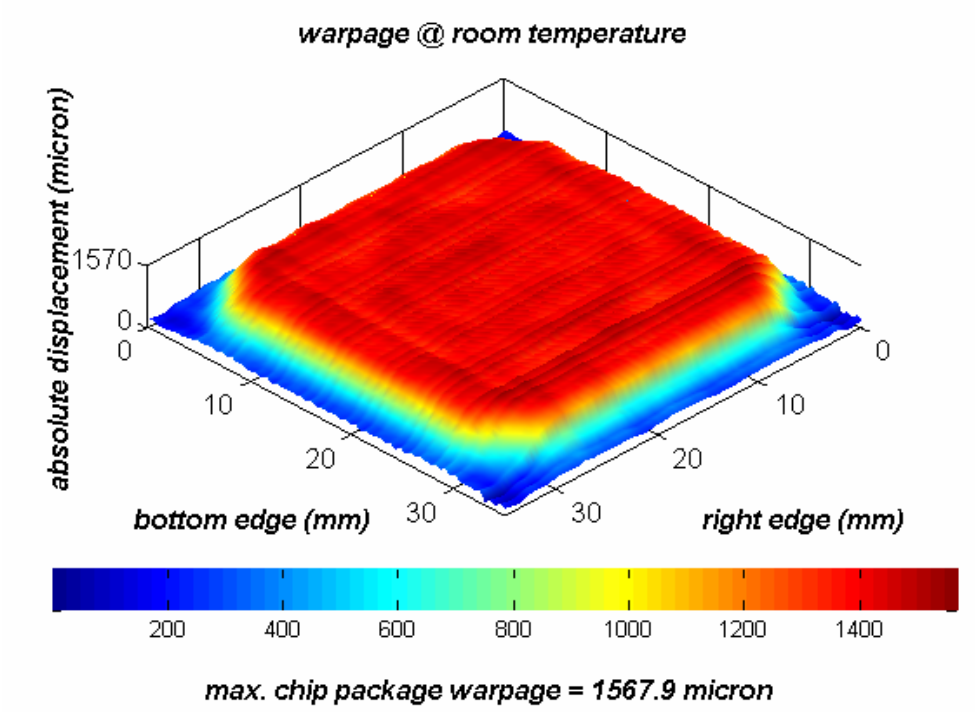


Figure 5.11. Out-of-plane displacement plot of 35 mm PBGA package

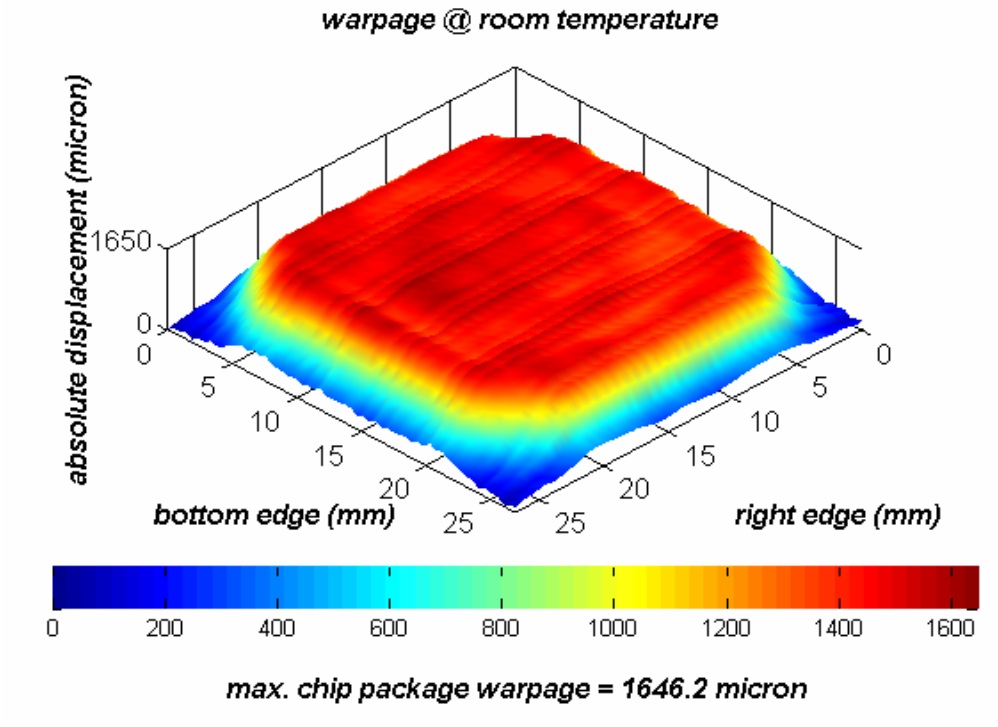


Figure 5.12. Out-of-plane displacement plot of 27 mm PBGA package

by measuring both PBGA packages using the projection moiré system. The PBGA packages were not assembled onto a PWB in Figure 5.11 and Figure 5.12. Note that the maximum warpage is the difference between the maximum and minimum out-of-plane displacements as described in Chapter 2. Figure 5.11 and Figure 5.12 show that the maximum warpage of the 35 mm PBGA package is 1567.9 microns and the maximum warpage of the 27 mm PBGA package is 1646.2 microns. Figure 5.13 shows an out-of-plane displacement plot of the PWB only. Figure 5.13 shows that maximum warpage of the PWB is 1854.5 microns.

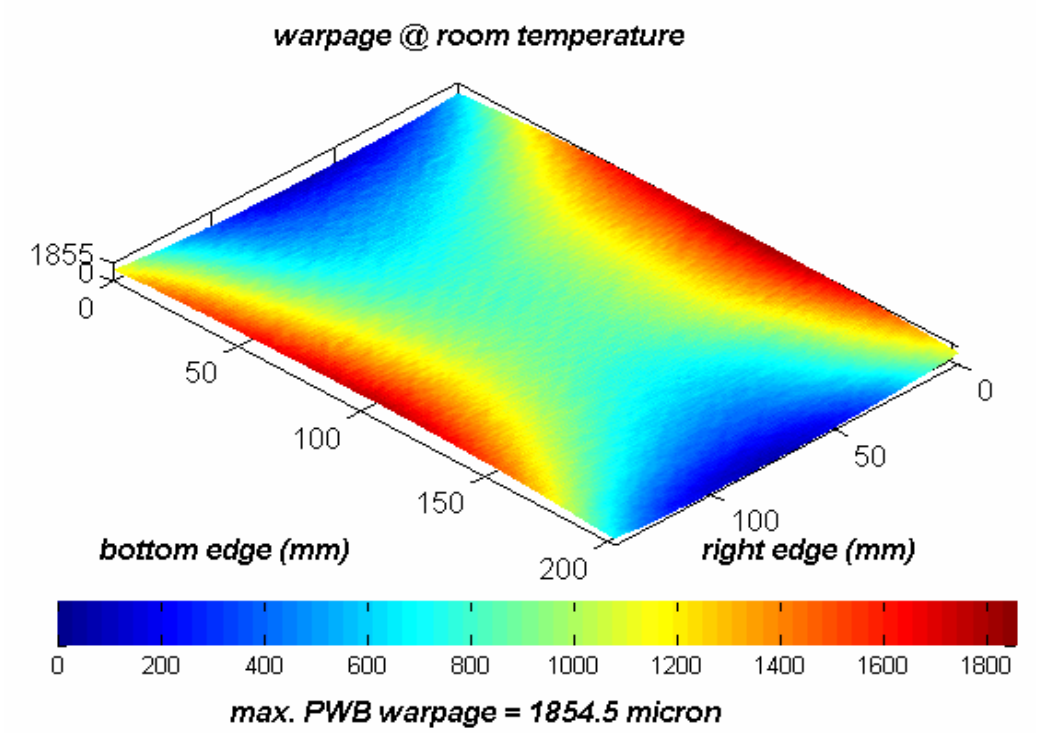


Figure 5.13. Out-of-plane displacement plot of 203.2 mm by 139.7 mm by 0.631 mm PWB

Next, the 35 mm PBGA package shown in Figure 5.11 is placed on the PWB shown in Figure 5.13 and then measured with the projection moiré system. The PBGA package is

placed on the lower right side of the PWB. Note that the chip package does not need to be permanently fixed to the PWB to demonstrate the automatic chip package detection algorithm. Figure 5.14 shows the initial snake that was constructed automatically using the automatic chip package detection algorithm. In Figure 5.14, the PBGA package is loosely placed on top of the PWB. Figure 5.14 shows that the PBGA package is contained entirely inside the initial contour which shows that the algorithm is able to find the PBGA package automatically. Figure 5.15 shows the snake after it has converged onto the edges of the PBGA package using the Greedy algorithm.

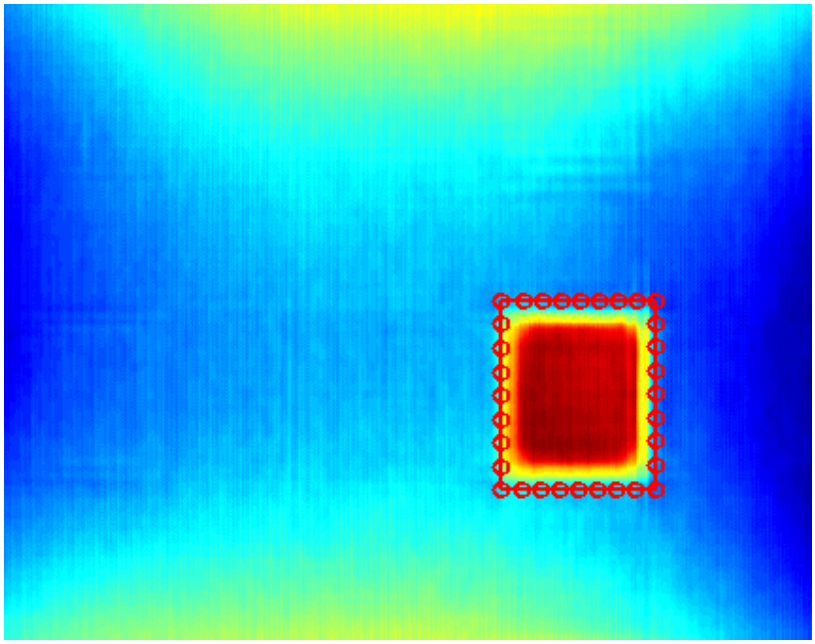


Figure 5.14. Initial snake constructed around a loose 35 mm PBGA package using automatic chip package detection algorithm

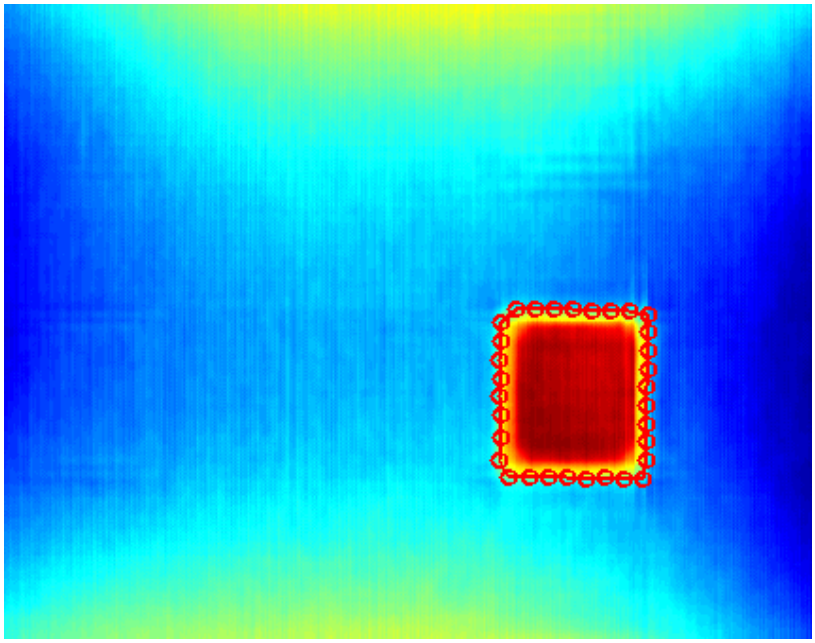


Figure 5.15. Converged snake for PWB with one loose 35 mm PBGA package

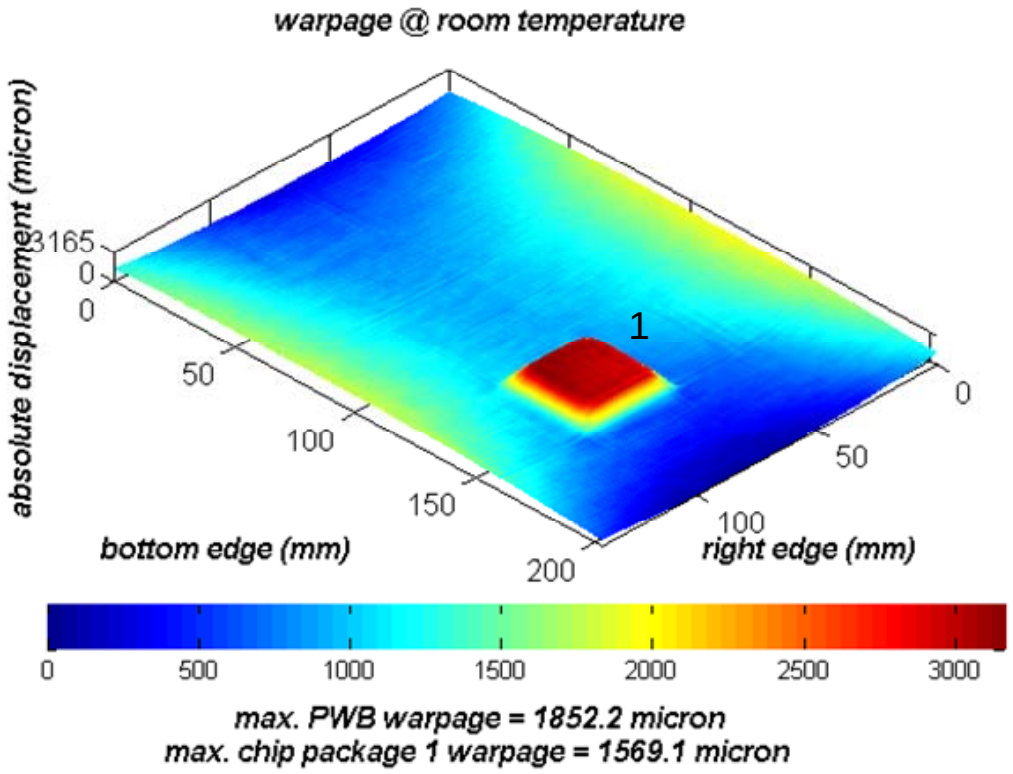


Figure 5.16. Out-of-plane displacement plot of PWB with one loose 35 mm PBGA package at lower right of PWB

The out-of-plane displacement plot of the PWB with one loose 35 mm PBGA package on the lower right side of the PWB is shown in Figure 5.16. Figure 5.16 shows that the measured maximum PWB warpage is 1852.2 microns and the maximum warpage of the 35 mm PBGA package is 1569.1 microns which is very close to the values obtained from measuring the PWB and 35 mm PBGA package separately as shown in Figure 5.11 and Figure 5.13 above. Before the chip package maximum warpage is calculated, a least squares rotation is performed on the chip package pixel values as described in Chapter 2. If a least squares rotation is not performed, the calculated chip package warpage result will include the warpage of the PWB underneath the chip package. The

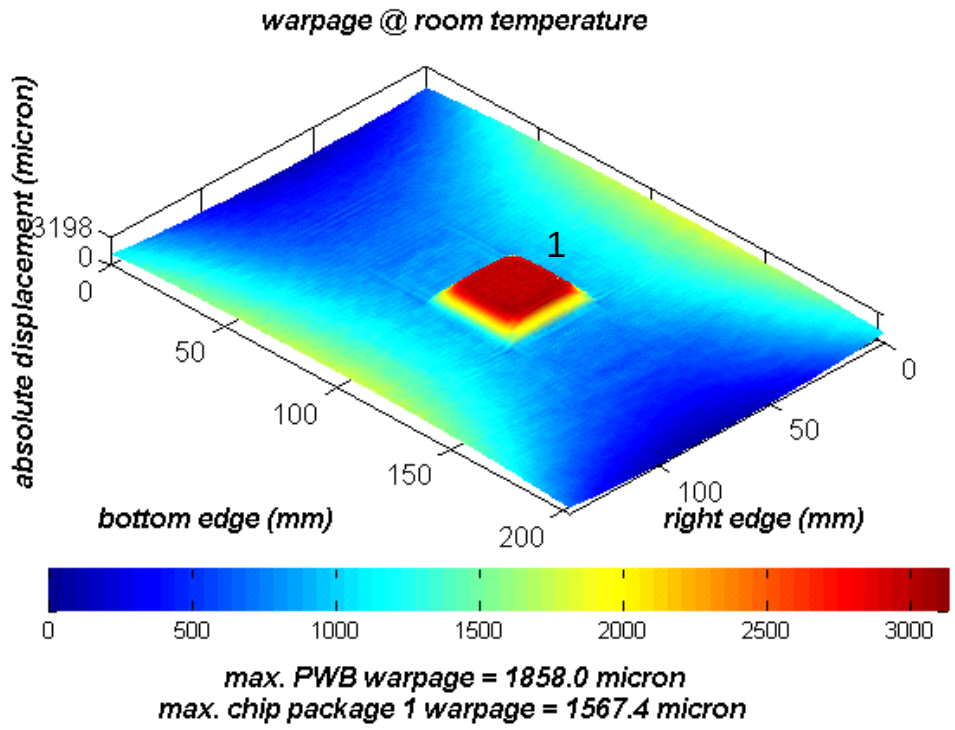


Figure 5.17. Out-of-plane displacement plot of PWB with one loose 35 mm PBGA package at lower right of PWB

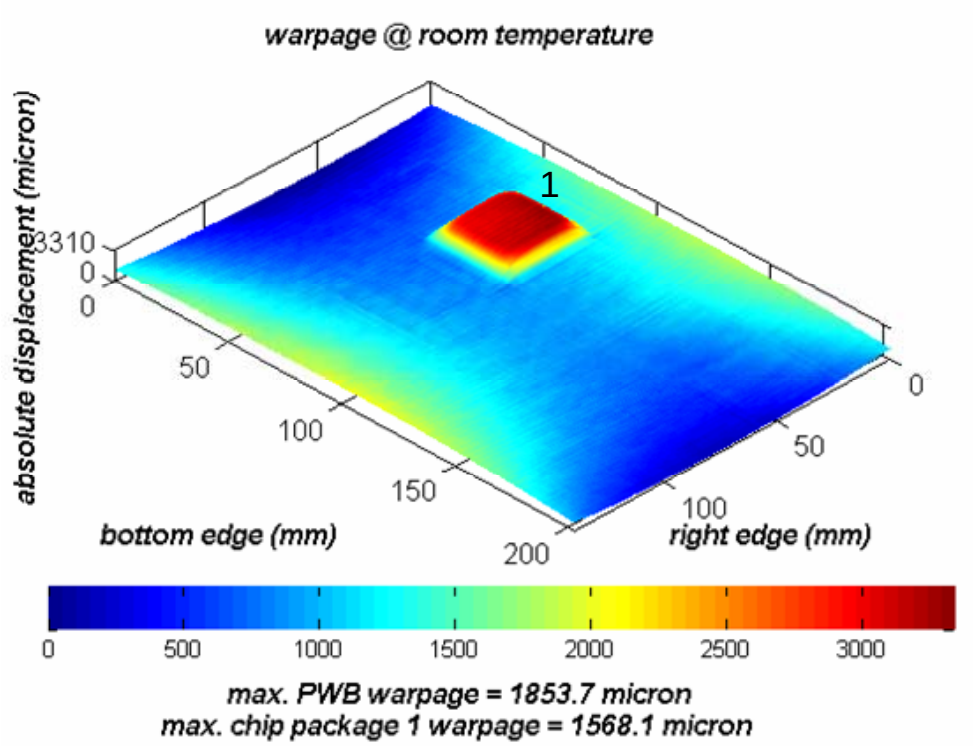


Figure 5.18. Out-of-plane displacement plot of PWB with one loose 35 mm PBGA package at lower right of PWB

35 mm PBGA package and the PWB were measured two more times with the PBGA package loosely placed in varying locations. Figure 5.17 shows the 35 mm PBGA package loosely placed in the center of the PWB and Figure 5.18 shows the 35 mm PBGA package loosely placed in the upper left corner of the PWB. Figure 5.17 shows that the maximum warpage of the PWB is 1858.0 microns and the maximum warpage of the PBGA package is 1567.4 microns. Figure 5.18 shows that the maximum warpage of the PWB is 1853.7 microns and the maximum warpage of the PBGA package is 1568.1 microns. Both figures show that the projection moiré can measure the maximum warpage of PWB and the 35 mm PBGA package accurately. Table 5.2 shows a comparison between the maximum warpage measurements of the loose 35 mm PBGA package in

Figures 5.19 to 5.20 when measured together with the PWB and the maximum warpage when measured alone as shown in Figure 5.11.

Table 5.2. Comparison between 35 mm PBGA package maximum warpage results when PBGA package measured on top of PWB with loose placement and when PBGA package measured alone

Figure Number	Maximum Warpage When 35 mm PBGA package Measured Alone (micron)	Maximum Warpage When PBGA Package With Loose Placement Measured with PWB (micron)	Percent Difference (%)
Figure 5.16	1567.9	1569.1	0.10
Figure 5.17	1567.9	1567.4	0.03
Figure 5.18	1567.9	1568.1	0.01

Table 5.2 shows that the projection moiré system can measure the maximum warpage of a PBGA package when measured simultaneously with a PWB. This is made possible by the automatic chip package detection algorithm discussed in this chapter. As shown in Table 5.2, when the 35 mm PBGA package is measured with the PWB, the measured maximum warpage value is very close to the maximum warpage obtained when the PBGA package is measured alone. The maximum percent difference obtained from these experiments was 0.10 %. Table 5.3 shows a comparison between the PWB maximum warpage results when the PWB was measured with the loose 35 mm PBGA package and when the PWB was measured alone. Table 5.3 shows that maximum percent difference was 0.20 %. Table 5.2 and Table 5.3 show that the projection moiré warpage measurement system can measure PWB and chip package warpage simultaneously just as well as measuring the PWB and chip package warpage separately.

Table 5.3. Comparison between PWB maximum warpage results when PWB measured with loose 35 mm PBGA package and when PWB measured alone

Figure Number	Maximum Warpage When PWB Measured Alone (micron)	Maximum Warpage When PWB Measured with One Loose PBGA Package (micron)	Percent Difference (%)
Figure 5.16	1854.5	1852.2	0.10
Figure 5.17	1854.5	1858.0	0.20
Figure 5.18	1854.5	1853.7	0.04

To show that the automatic chip package detection algorithm implemented in this research can be used for PWBAs for more than one chip package, the projection moiré system was used to measure the PWB with the 35 mm PBGA package and the 27 mm PBGA package presented earlier positioned loosely on top of the PWB. Figure 5.19 shows the initial snakes around the loose 27 mm PBGA package and the loose 35 mm PBGA package constructed using the automatic chip package detection algorithm. The

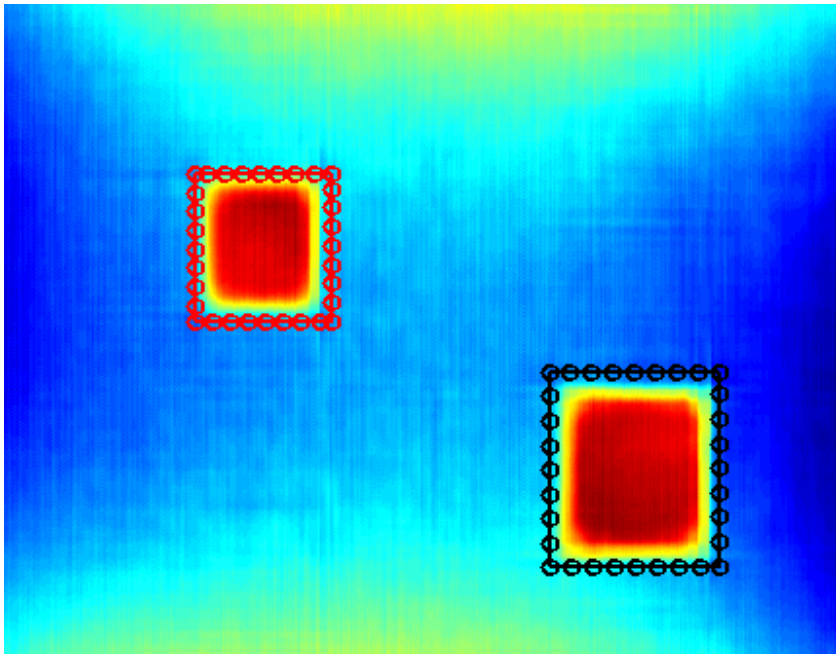


Figure 5.19. Initial snake constructed around loose 27 mm and loose 35 mm PBGA packages using automatic chip package detection algorithm

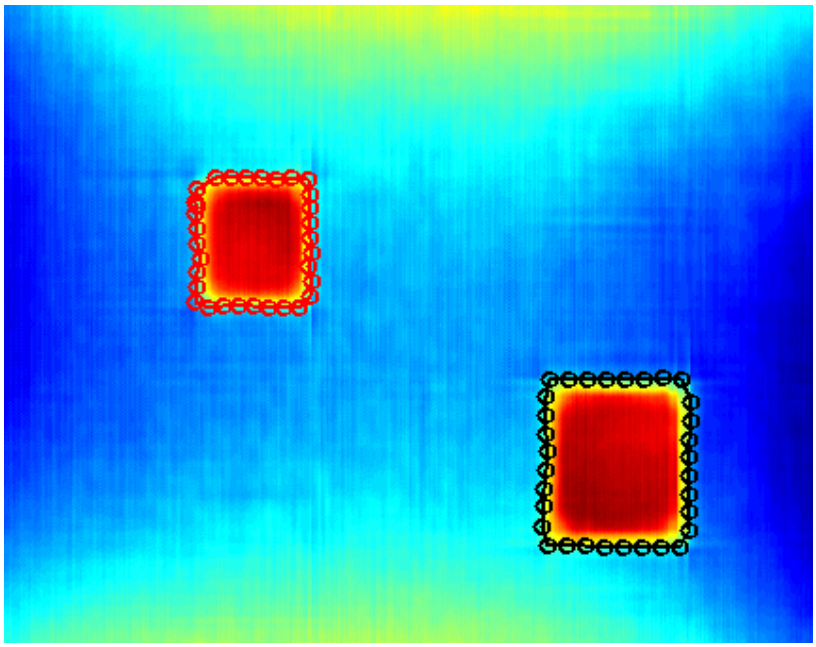


Figure 5.20. Converged snake for PWB with one loose 27 mm PBGA pckage and one loose 35 mm PBGA package

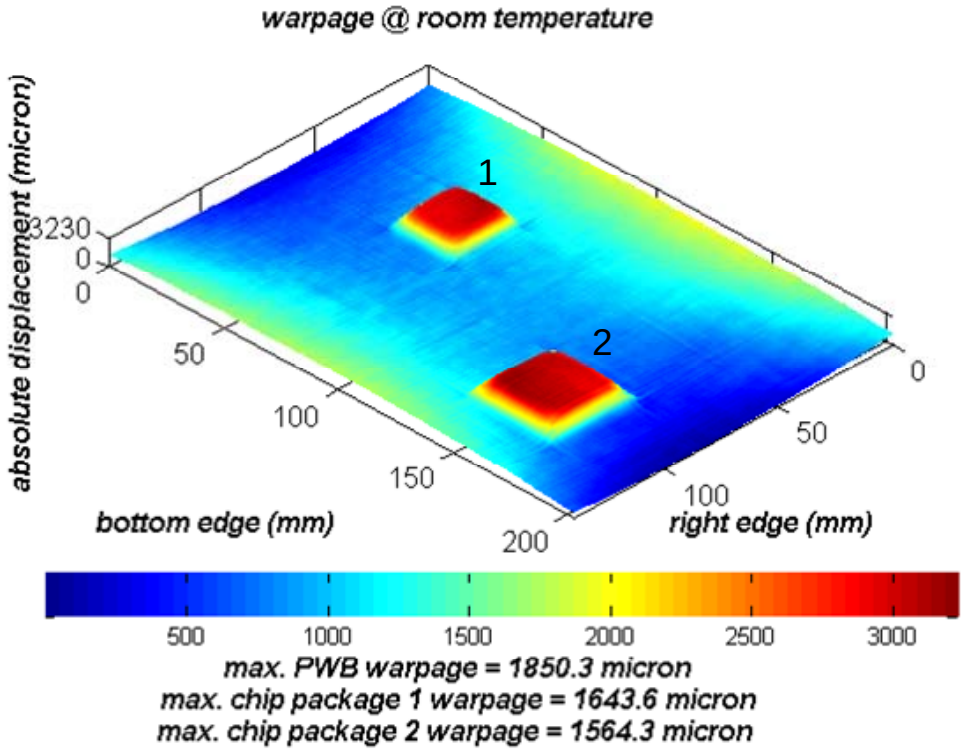


Figure 5.21. Out-of-plane displacement plot of PWB with one loose 35 mm PBGA package at bottom right and one loose 27 mm PBGA package at top left of PWB

converged snakes for the two loose PBGA packages are shown in Figure 5.20. Figure 5.19 and Figure 5.20 show that the automatic chip package detection algorithm can be used to detect more than one PBGA package. The out-of-plane displacement plot of the PWBA corresponding to Figure 5.19 and Figure 5.20 is shown in Figure 5.21. Figure 5.21 shows that the measured maximum warpage of the PWB was 1850.3 microns. The measured maximum warpage of the loose 27 mm PBGA package was 1643.6 micron and the maximum warpage of the loose 35 mm PBGA package was 1564.3 microns. The projection moiré system was used to measure a PWB with the loose 27 mm PBGA package and the loose 35 mm PBGA package in another configuration. Figure 5.22 shows the out-of-plane displacement plot of the PWB with loose 27 mm PBGA package

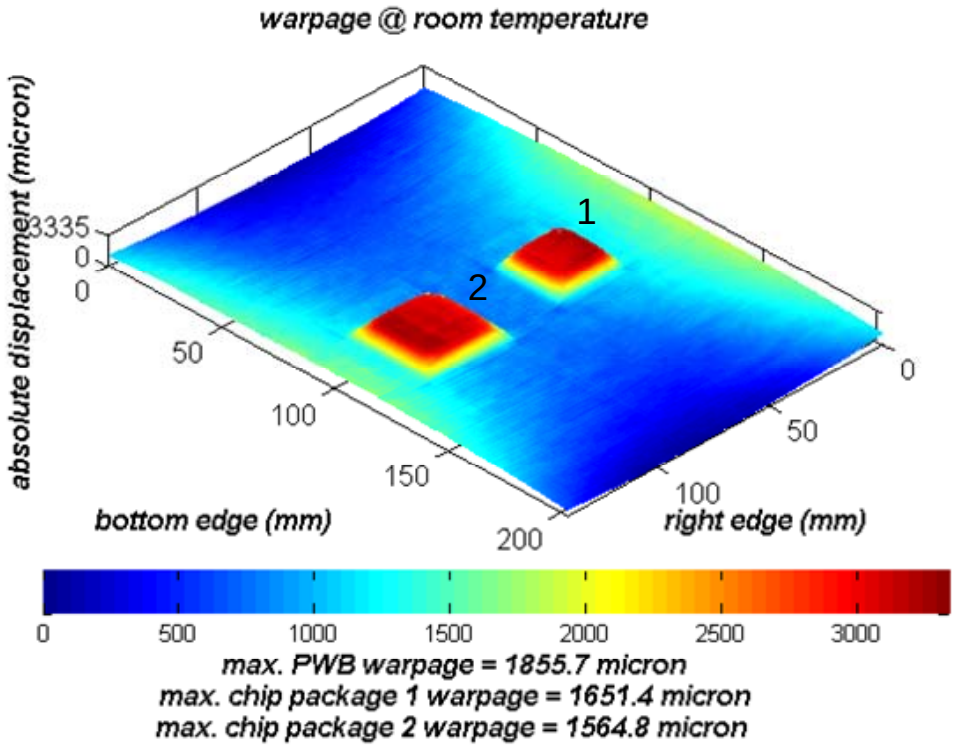


Figure 5.22. Out-of-plane displacement plot of PWB with one loose 35 mm PBGA package at bottom center of PWB and one loose 27 mm PBGA package at top center of PWB

at the top center of the PWB and the loose 35 mm PBGA chip package and the bottom center of the PWB. Figure 5.22 shows that the measured maximum warpage of the PWB was 1855.7 microns. The measured maximum warpage of the loose 27 mm PBGA package was 1651.4 microns and the measured maximum warpage of the loose 35 mm PBGA package was 1564.8 microns. Table 5.4 shows a comparison between the 27 mm PBGA package maximum warpage results when the 27 mm PBGA package is measured with the 35 mm PBGA package loosely placed on top of the PWB and when the 27 mm PBGA package is measured alone. Table 5.4 shows that the maximum percent difference for the comparison was 0.32 %.

Table 5.4. Comparison between 27 mm PBGA package maximum warpage results when 27 mm PBGA package measured with 35 mm PBGA package both loosely placed on top of PWB and when 27 mm PBGA package measured alone

Measurement Number	Maximum Warpage When 27 mm PBGA package Measured Alone (micron)	Maximum Warpage When 27 mm PBGA Package Measured with Loose Placement on PWB Along with Loosely Placed 35 mm PBGA Package (micron)	Percent Difference (%)
Figure 5.21	1646.2	1643.6	0.16
Figure 5.22	1646.2	1651.4	0.32

Table 5.5 shows a comparison between the 35 mm PBGA package maximum warpage results when the 35 mm PBGA package is measured with the 27 mm PBGA both loosely

Table 5.5. Comparison between 35 mm PBGA package maximum warpage results when 35 mm PBGA package measured with 27 mm PBGA package both loosely placed on top of PWB and when 35 mm PBGA package measured alone

Measurement Number	Maximum Warpage When 35 mm PBGA package Measured Alone (micron)	Maximum Warpage When 35 mm PBGA Package Measured with Loose Placement on PWB Along with Loosely Placed 27 mm PBGA package (micron)	Percent Difference (%)
Figure 5.21	1567.9	1564.3	0.23
Figure 5.22	1567.9	1564.8	0.20

placed on top of the PWB and when the 35 mm PBGA package is measured alone. Table 5.5 shows that the maximum percent difference for the comparison was 0.23 %.

Table 5.6 shows a comparison between the PWB maximum warpage results when the PWB is measured with the loose 27 mm PBGA and the loose 35 mm PBGA package and when the PWB is measured alone. Table 5.6 shows that the maximum percent difference for the comparison was 0.23 %.

Table 5.6. Comparison between PWB maximum warpage results when PWB measured with 27 mm PBGA package and 35 mm PBGA package both loosely placed on top of PWB and when PWB measured alone

Measurement Number	Maximum Warpage When PWB Measured Alone (micron)	Maximum Warpage When PWB Measured with Loosely Placed 27 mm PBGA package and Loosely Placed 35 mm PBGA Package (micron)	Percent Difference (%)
Figure 5.21	1854.5	1850.3	0.23
Figure 5.22	1854.5	1855.7	0.06

Tables 5.4 to 5.6 show that the projection moiré warpage measurement system can measure PWB and more than one PBGA package maximum warpage simultaneously just as well as measuring the maximum warpage of the PWB and chip packages separately. It should be noted that since the length of the PWB measured in this chapter is 203.2 mm, the resolution provided by the projection moiré system is 20.32 microns. Since the results presented are are within the resolution of the measurement, the exact percent difference values may be questionable. However, the results still show that there is good agreement between measurements of PWBs and PBGA packages when the PWB and PBGA package(s) are measured alone or when they are measured together with the PBGA package(s) loosely placed on the PWB. The algorithm developed in this research will now allow the projection moiré system to measure and calculate the maximum warpage of populated PWBs.

5.4 Limitations of Automatic Chip Package Detection Algorithm

The currently implemented chip package detection algorithm only works for PWBAs with up to two chip packages. The MATLAB program is very modular and making the algorithm work for more than two chip packages would simply require code repetition. However, for PWBs populated with several chip packages, code repetition may not be the most efficient way of implementing the algorithm. The currently implemented chip package detection algorithm also only works for chip packages whose edges are oriented in the vertical and horizontal directions with the respect to the edges of the PWB. In some PWBAs, chip packages are oriented at 45 degree angles to the edges of the PWB. To handle these cases, the part of the algorithm that constructs the initial

snake must be modified. Also, the algorithm may not be perfectly accurate if the maximum or minimum PWB out-of-plane displacement occurs directly underneath the chip package of interest. To show that there is no significant loss in accuracy when the minimum or maximum out-of-plane displacement occurs underneath the chip package, a finite element plot is used to demonstrate this scenario. Figure 5.23 shows an out-of-plane displacement plot of a PWB with one PBGA package at its center. For this case, the minimum out-of-plane displacement occurs directly underneath the PBGA package. The

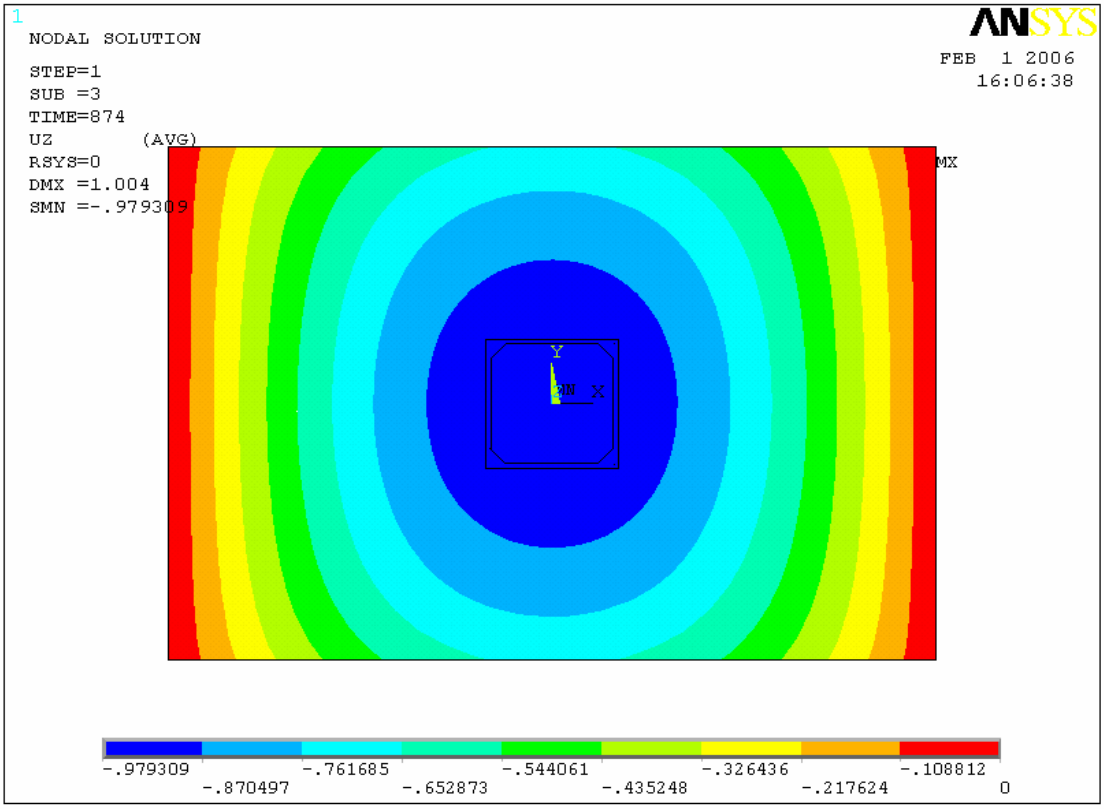


Figure 5.23. Out-of-plane PWB displacement plot of PWB with one PBGA at its center obtained from FE model

minimum PWB out-of-plane displacement shown in Figure 5.23 is -0.9793 mm and the maximum out-of-plane displacement is 0 mm if we assume that the maximum and minimum values occurs at the bounds of the colormap. Therefore, the maximum PWB warpage is 0.9793 mm. If the location of the PBGA package is not used in the calculation, the minimum out-of-plane displacement becomes -0.9428 mm, which represents a maximum PWB warpage value of 0.9428 mm. The difference between the two cases is 3.7 %, so the method implemented in this dissertation is valid. However, one possible way to tackle the problem of the maximum or minimum out-of-plane displacements occurring underneath the chip package is to use the converged snake to construct a surface patch on the PWB in the location of the chip package. The surface patch would be used to approximate the PWB deformation underneath the chip package.

Another limitation of the automatic chip package detection algorithm is that if the chip packages are placed less than approximately 10 mm of each other, the algorithm may generate erroneous results. This is because the chip package detection algorithm determines that it has found the bounding coordinates of the chip package when it sees three zeros in a row.

5.5 Projection Moiré System Repeatability Study

A repeatability study was performed on the projection moiré measurement system to determine it's suitability for online measurements. In order for the system to be reliable, it must produce repeatable measurements. The repeatability study was conducted by measuring the maximum warpage of an unpopulated PWB at room temperature using the projection moiré system. The experiment was repeated 10 times using the same

sample. The sample was not moved nor was the setup recalibrated between measurements. The maximum warpage results of the 10 runs as well as the average and standard deviation are shown in Table 5.7 below.

Table 5.7. PWB warpage measurements for repeatability study

Measurement Number	**Measured Maximum PWB Warpage (microns)**
1	2015.9
2	2014.8
3	2030.5
4	2008.5
5	2023.0
6	2017.5
7	2009.3
8	2027.6
9	2035.1
10	2020.4
AVERAGE	**2020.3**
STANDARD DEVIATION	**8.8**

In order to calculate the repeatability, the confidence interval for one measurement point must be calculated. Confidence interval is defined by Equation (5.10).

$$CI = x_m \pm z\left(\frac{\alpha}{2}\right)\frac{\sigma}{\sqrt{n}} \tag{5.10}$$

where,

CI = confidence interval of measurement

x_m = average of observations

$z(\alpha/2)$ = 2.0 for 95^{th} percentile confidence interval (based on normal distribution of data)

σ = standard deviation of observations

n = number of observations

From the results shown in Table 5.7 and using Equation (5.10), the confidence interval for one measurement is:

$$CI = 2020.3 \pm (2)\left(\frac{8.8}{\sqrt{1}}\right) \ microns$$

$$CI = 2020.3 \pm 17.6 \ microns$$

The repeatability is determined by dividing the tolerance by the mean of the confidence interval. Therefore, the repeatability of the projection moiré measurement is 17.6/2020.3 which is equal to 0.9 %. In measurement system analysis, usually, the repeatability is acceptable if it is less than 10 %. Since the projection moiré system has a repeatability significantly less than 10 %, the system has excellent repeatability.

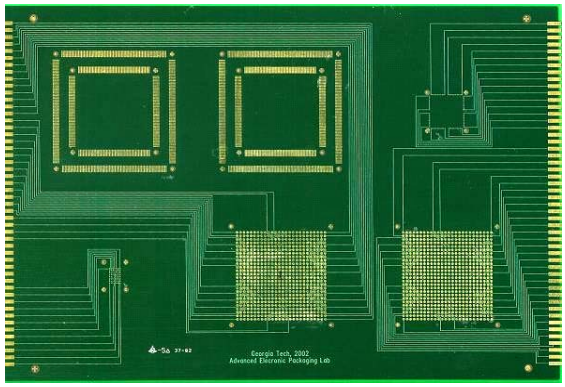
CHAPTER 6

PROJECTION MOIRÉ WARPAGE STUDIES OF PWBS POPULATED WITH PBGA PACKAGES

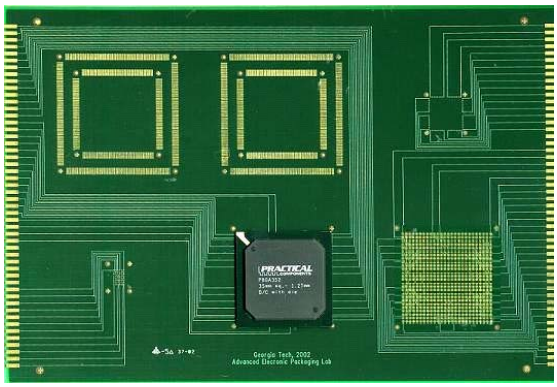
The third objective of this research was to utilize the convective reflow projection moiré system to study the warpage of PWBA test vehicles. The goal of the present study is to assess the effect of PBGA packages on PWB warpage. The test vehicle is discussed next.

6.1 Measurement Test Vehicle

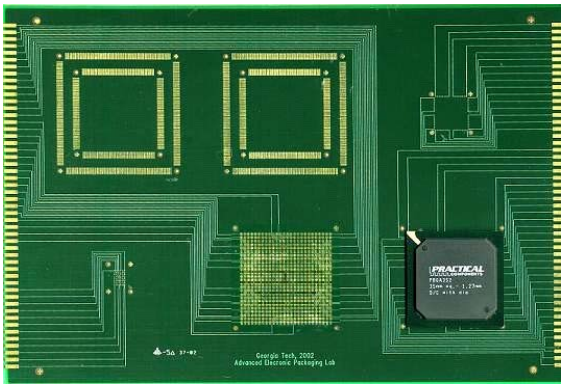
The PWBA test vehicle that will be used in this study is a 203.2 mm by 139.7 mm by 0.631 mm four layer PWB that can accommodate various surface mount electronic components which was first developed by Hai Ding [18]. Specifically, the PWB is comprised of one layer of copper-clad FR4, two layers of FR4 core laminate, and two layers of copper. The copper layers are 18-μm thick half-ounce copper foils. The top copper layer of the PWB contains traces, which are 127-μm thick and have a pitch of 508-μm. The surface finish of the substrate bond pads is electroless nickel/immersion gold. The PWBA test vehicle is shown in Figure 6.1.



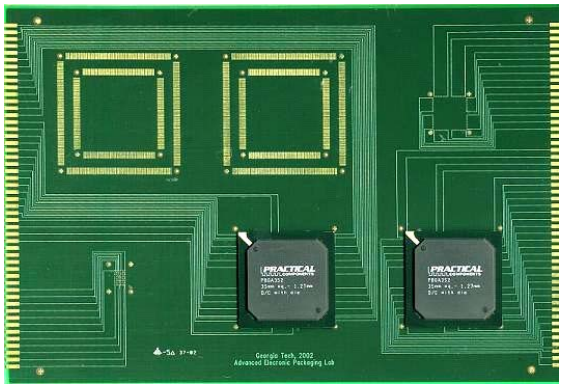
Configuration 1



Configuration 2



Configuration 3



Configuration 4

Figure 6.1. PWBA test vehicle in four configurations

6.2 Test Vehicle Measurement Approach

The projection moiré system was used to measure the PWB/PWBA test vehicle in four configurations. To define the configurations, the origin is located at the center of the PWB. The x-axis is along the length of the PWB and the y-axis is along the width of the PWB. The four configurations are shown in Figure 6.1. Configuration 1 conists of the bare PWB. Configuration 2 consists of the PWB with one 35 mm PBGA package located a distance of 30 mm in the negative y-direction from the PWB origin. Configuration 3 consists of the PWB with one 35 mm PBGA package located a distance of 60 mm in the positive x-direction and 30 mm in the negative y-direction from the PWB origin. Configuration 4 consists of the PWB with one 35 mm PBGA package located a distance

of 30 mm in the negative y-direction from the PWB origin and one 35 mm PBGA package located a distance of 60 mm in the positive x-direction and 30 mm in the negative y-direction from the PWB origin. Note that there are only two possible PBGA package assembly locations on the test vehicle. The PWB/PWBA is supported in the oven chamber by invar rails along the left and right short edges of the PWB. The four configurations of the PWBA were measured during a convective heating process. For each configuration, the projection moiré technique was used to measure the warpage of the PWBA at initial room temperature, 140 ^{o}C heating, 210 ^{o}C, 140 ^{o}C cooling and final room temperature. The temperatures 140 ^{o}C and 210 ^{o}C were chosen

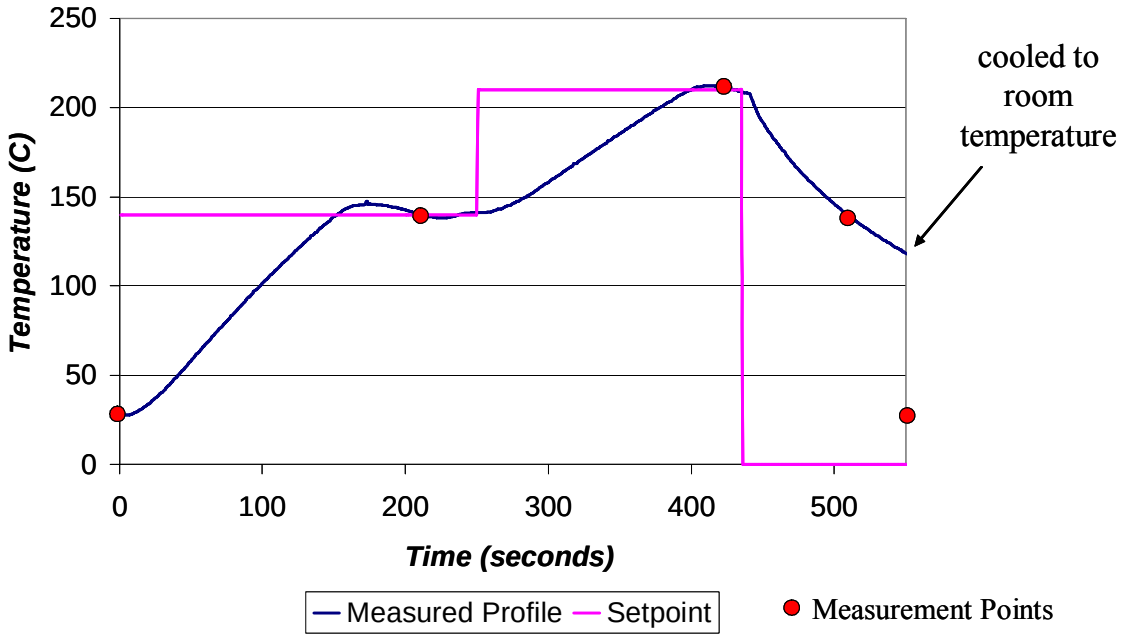


Figure 6.2. Input and measured convective temperature profile for PWBA projection moiré warpage experiments

because they respresent typical soak and peak temperatures for standard RDRP profiles for eutectic solder. Constant temperature setpoints of 140 ^{o}C and 210 ^{o}C were input to the

temperature controller such that the convective system would heat the PWBA as fast as possible. Figure 6.2 below shows the input constant setpoints and measured temperature profile of the bare PWB.

6.3 PWBA Test Vehicle Warpage Measurement Results

The measured warpage results of PWB Configuration 1 at initial room temperature, 140 ^{o}C heating, 210 ^{o}C, 140 ^{o}C cooling and final room temperature are shown in Figure 6.3 to Figure 6.7. The out-of-plane displacement plots show that the PWB warped in a concave upward shape. The initial PWB maximum warpage before heating was 2158.9 microns. As the PWB was heated, the PWB maximum warpage reduced to 1513.8 microns at 140 ^{o}C and to 967.5 microns at the peak temperature of 210 ^{o}C. As the PWB was cooled back to room temperature the PWB maximum warpage increased to 1669.3 microns at 140 ^{o}C and to 2292.6 microns at room temperature. The maximum warpage results of PWB Configuration 1 also showed that the PWB warped in a largely symmetric fashion but not always so due the effects of traces which are not symmetric as shown in Figure 6.1

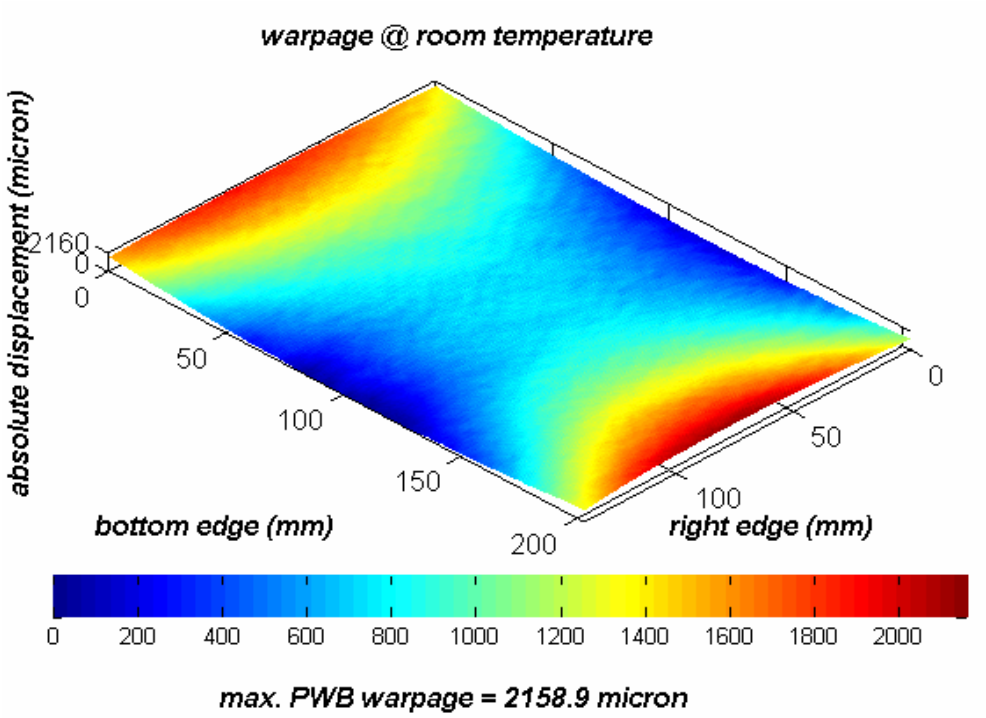


Figure 6.3. Out-of-plane displacement plot of PWBA Configuration 1 at initial room temperature

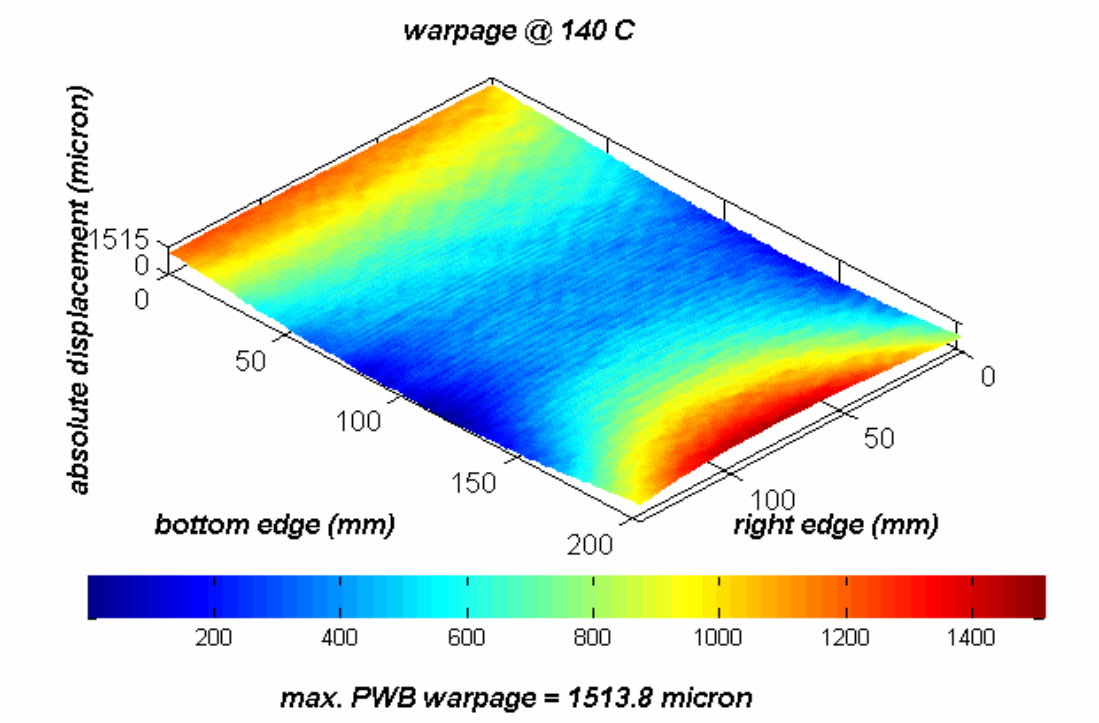


Figure 6.4. Out-of-plane displacement plot of PWBA Configuration 1 at 140 ^{o}C heating

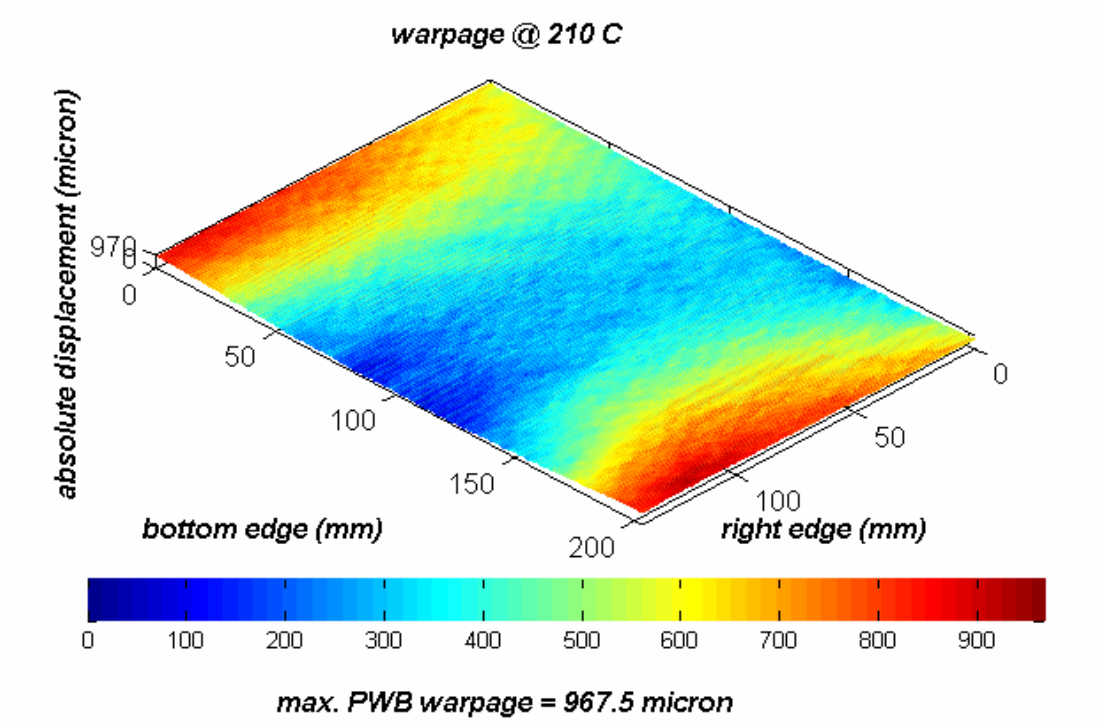


Figure 6.5. Out-of-plane displacement plot of PWBA Configuration 1 at 210 ^{o}C peak temperature

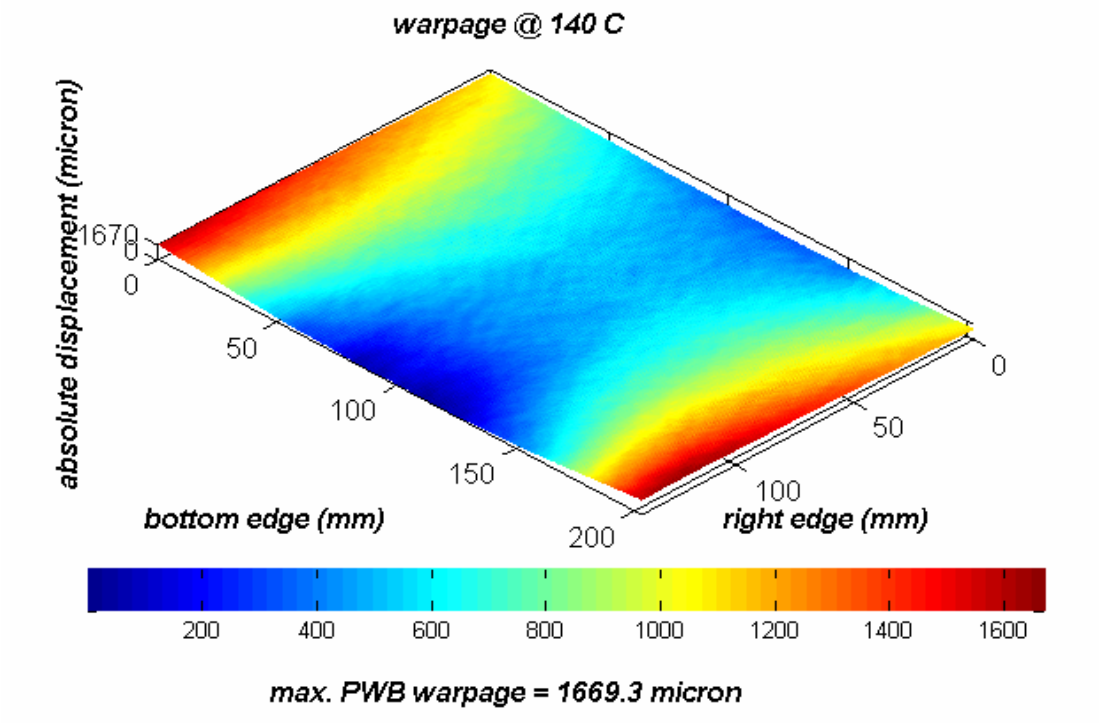


Figure 6.6. Out-of-plane displacement plot of PWBA Configuration 1 at 140 ^{o}C cooling

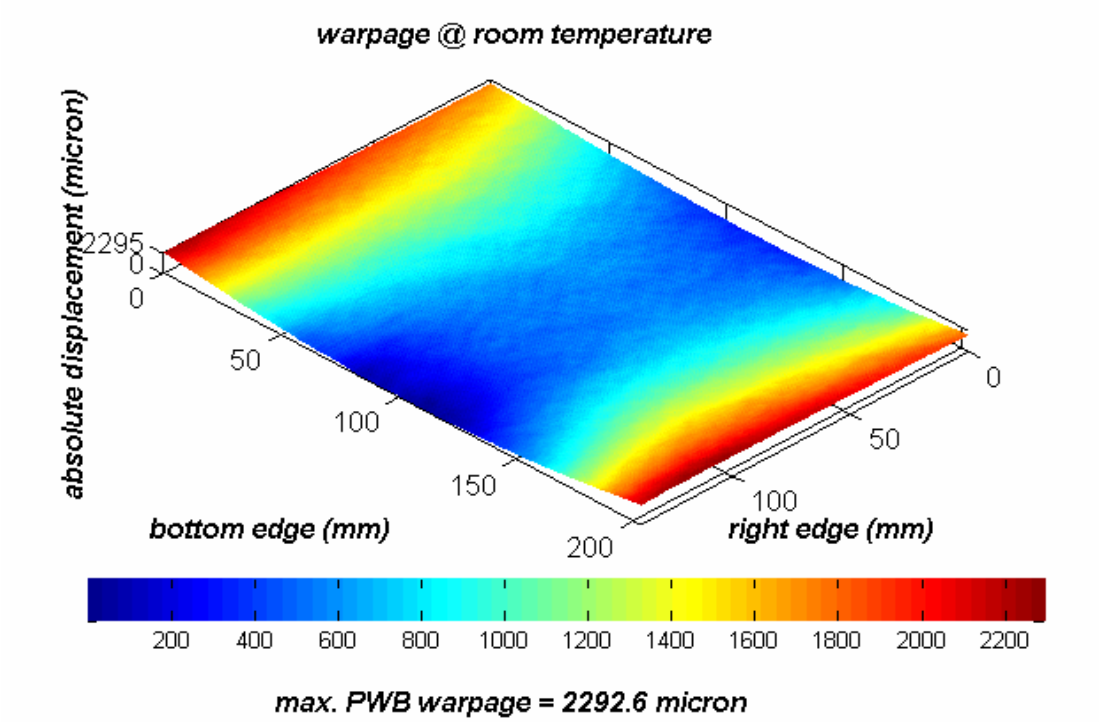


Figure 6.7. Out-of-plane displacement plot of PWBA Configuration 1 at final room temperature

The measured warpage results of PWB Configuration 2 at initial room temperature, 140 ^{o}C heating, 210 ^{o}C, 140 ^{o}C cooling and final room temperature are shown in Figure 6.8 to Figure 6.12. The out-of-plane displacement plots show that the PWB warped in a concave upward shape. The initial PWB maximum warpage before heating was 2256.2 microns. As the PWB was heated, the PWB maximum warpage reduced to 1438.9 microns at 140 ^{o}C and to 1289.4 microns at the peak temperature of 210 ^{o}C. As the PWB was cooled back to room temperature the PWB maximum warpage increased to 1885.3 microns at 140 ^{o}C and to 2396.1 microns at room temperature. The maximum warpage results of PWB Configuration 2 also showed that the PWB warped in a largely symmetric fashion but not always so due the effects of traces which are not symmetric as shown in Figure 6.1.

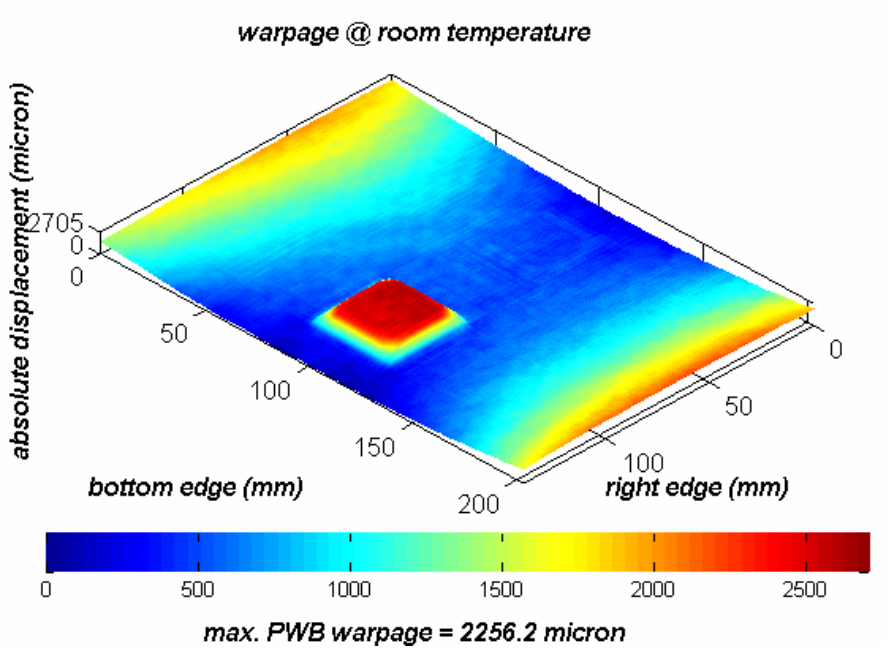


Figure 6.8. Out-of-plane displacement plot of PWBA Configuration 2 at initial room temperature

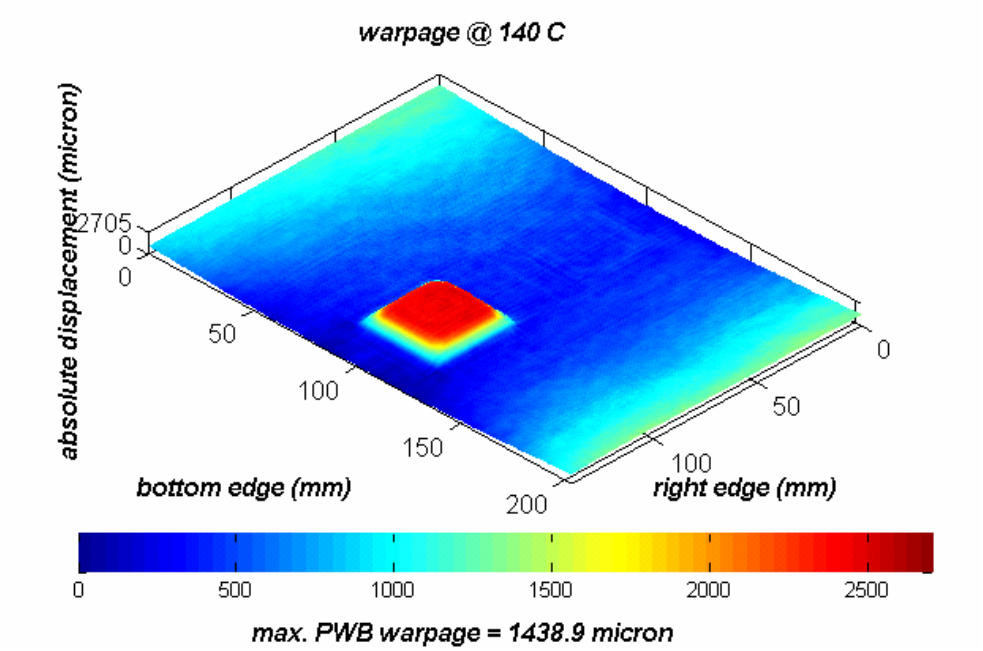


Figure 6.9. Out-of-plane displacement plot of PWBA Configuration 2 at 140 ^{o}C heating

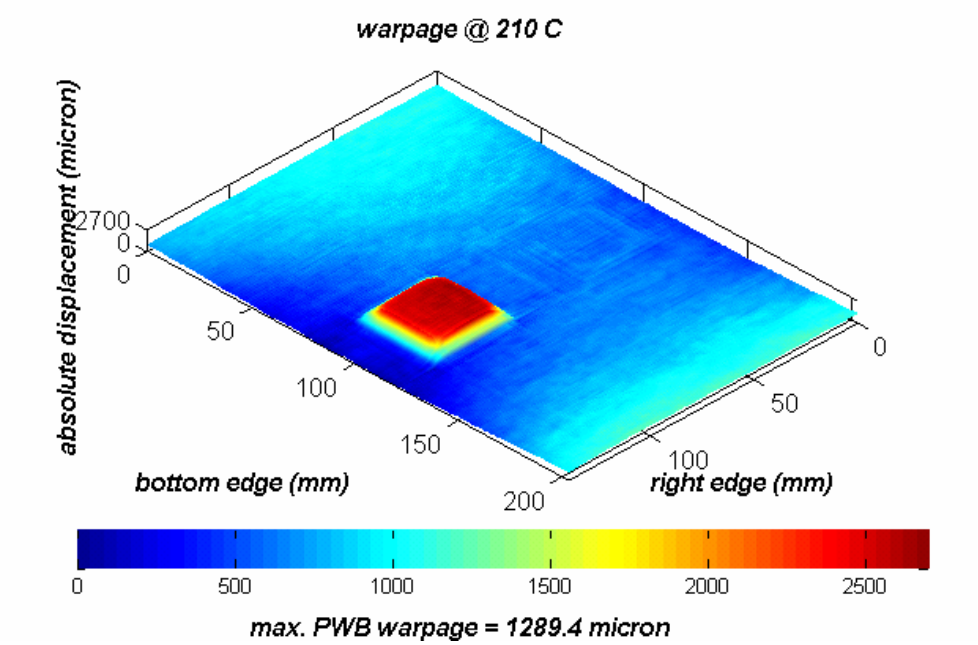


Figure 6.10. Out-of-plane displacement plot of PWBA Configuration 2 at 210 ^{o}C

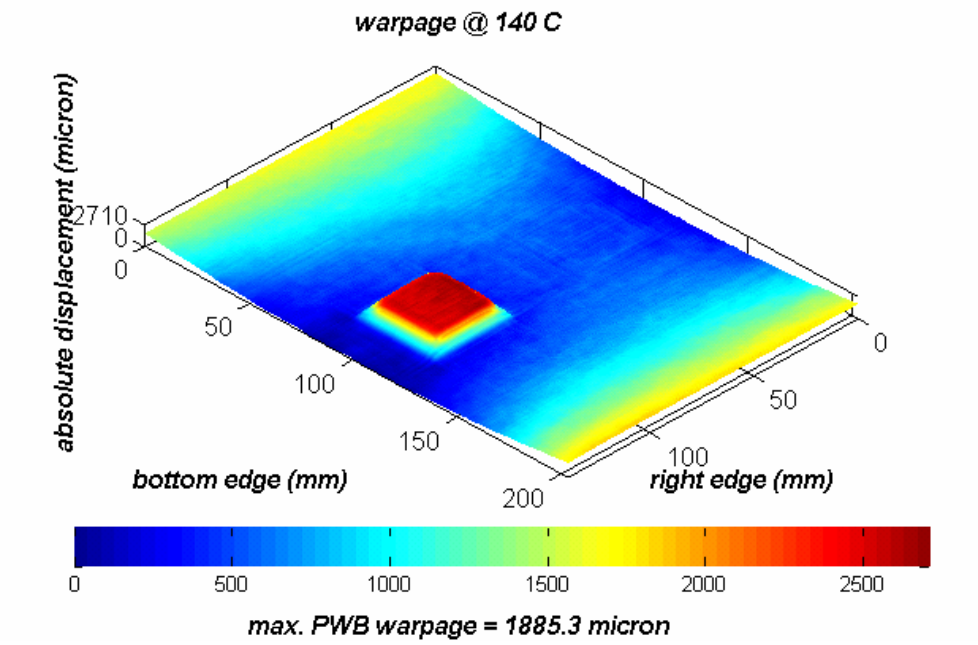


Figure 6.11. Out-of-plane displacement plot of PWBA Configuration 2 at 140 ^{o}C cooling

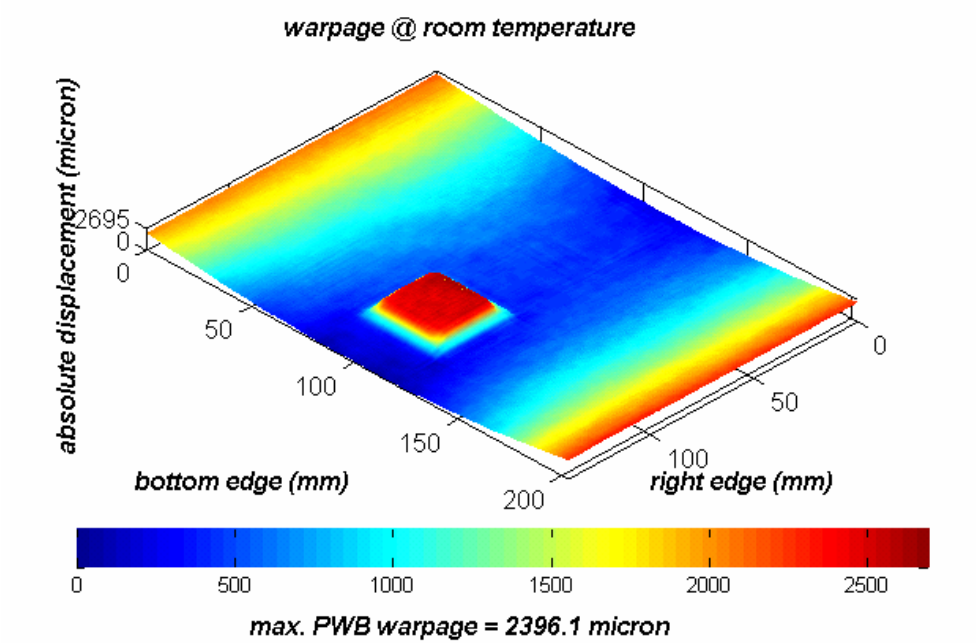


Figure 6.12. Out-of-plane displacement plot of PWBA Configuration 2 at final room temperature

The measured warpage results of PWB Configuration 3 at initial room temperature, 140 ^{o}C heating, 210 ^{o}C, 140 ^{o}C cooling and final room temperature are shown in Figure 6.13 to Figure 6.17. The out-of-plane displacement plots show that the PWB warped in a concave upward shape. The initial PWB maximum warpage before heating was 2175.8 microns. As the PWB was heated, the PWB maximum warpage reduced to 1742.0 microns at 140 ^{o}C and to 1624.4 microns at the peak temperature of 210 ^{o}C. As the PWB was cooled back to room temperature the PWB maximum warpage increased to 2317.6 microns at 140 ^{o}C and to 2660.3 microns at room temperature. The maximum warpage results of PWB Configuration 3 also showed that the PWB did not warp symmetrically even though it retained a concave upward shape.

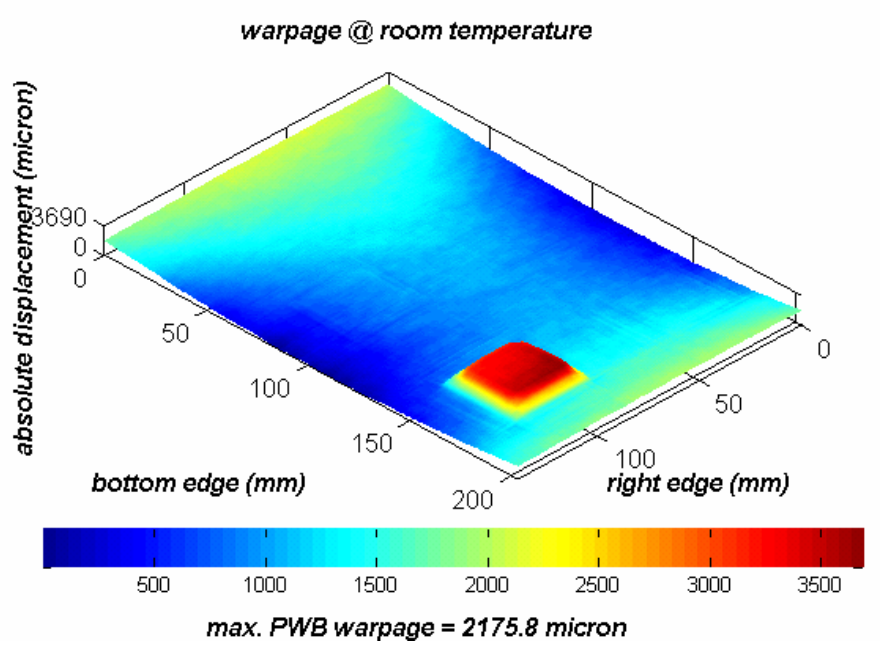


Figure 6.13. Out-of-plane displacement plot of PWBA Configuration 3 at initial room temperature

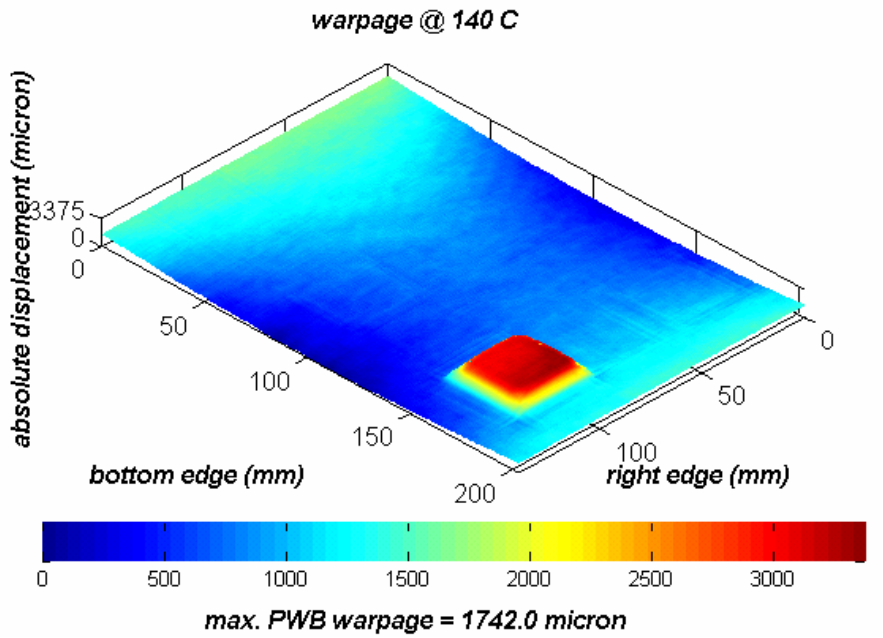


Figure 6.14. Out-of-plane displacement plot of PWBA Configuration 3 at 140 ^{o}C heating

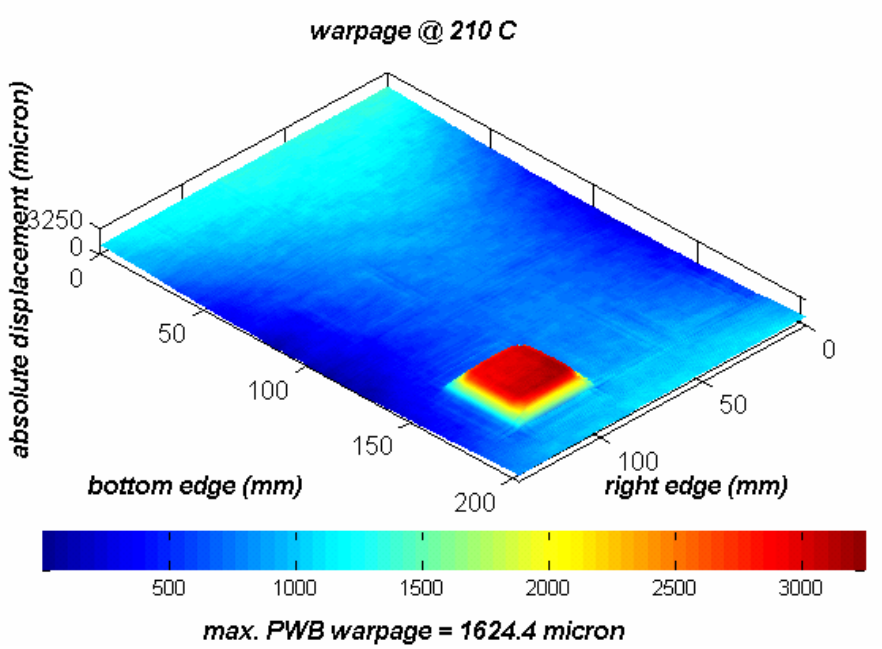


Figure 6.15. Out-of-plane displacement plot of PWBA Configuration 3 at 210 ^{o}C

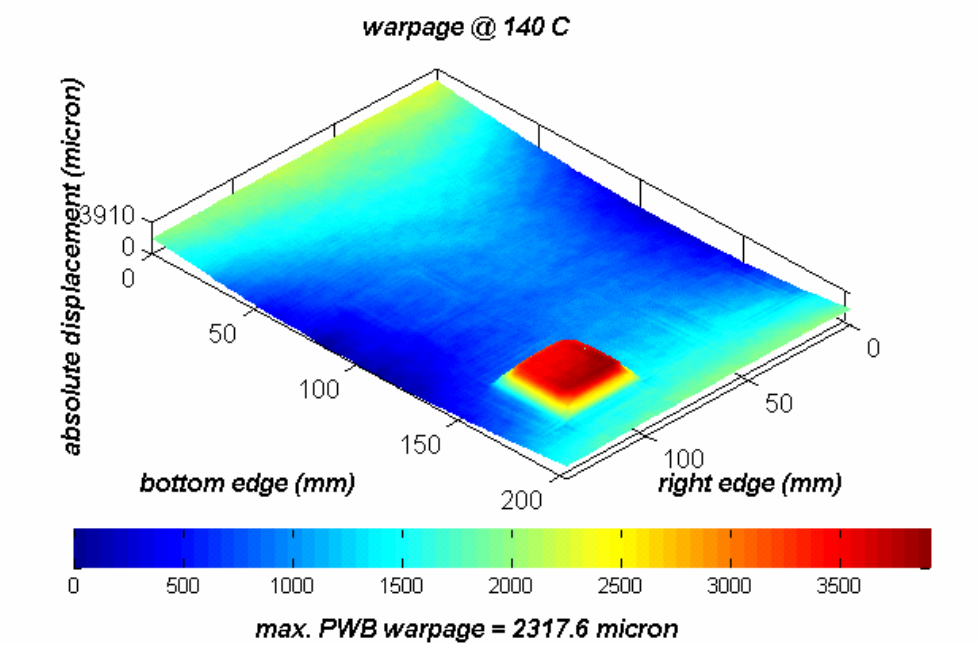


Figure 6.16. Out-of-plane displacement plot PWBA Configuration 3 at 140 ^{o}C cooling

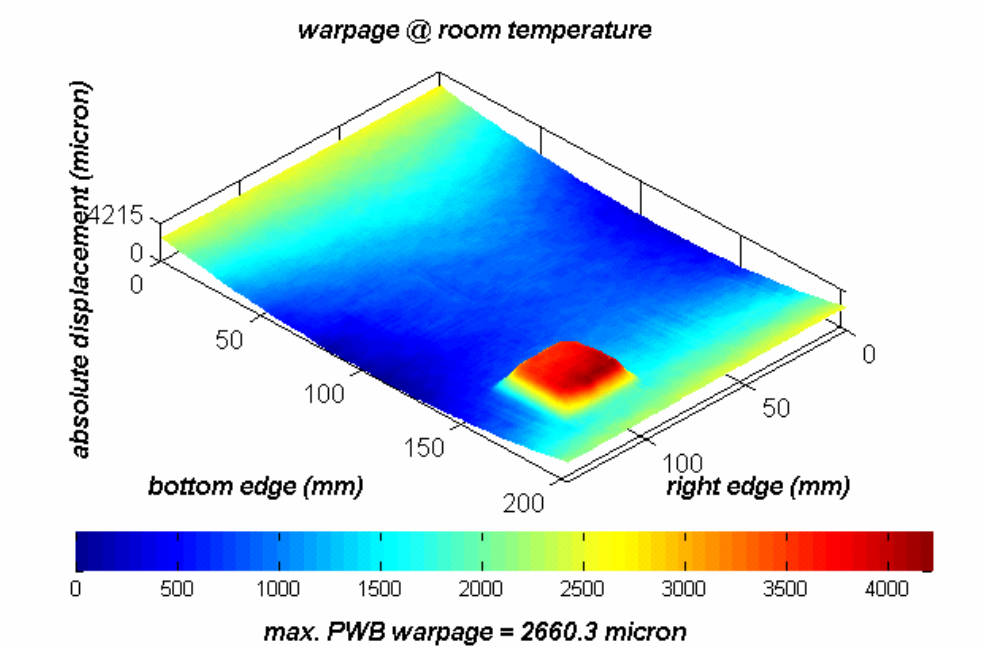


Figure 6.17. Out-of-plane displacement plot PWBA Configuration 3 at final room temperature

The measured warpage results of PWB Configuration 4 at initial room temperature, 140 ^{o}C heating, 210 ^{o}C, 140 ^{o}C cooling and final room temperature are shown in Figure 6.18 to Figure 6.22. The out-of-plane displacement plots show that the PWB warped in a concave upward shape. The initial PWB maximum warpage before heating was 2102.8 microns. As the PWB was heated, the PWB maximum warpage reduced to 2037.1 microns at 140 ^{o}C and to 1793.3 microns at the peak temperature of 210 ^{o}C. As the PWB was cooled back to room temperature the PWB maximum warpage increased to 2272.0 microns at 140 ^{o}C and to 2580.7 microns at room temperature. The maximum warpage results of PWB Configuration 4 showed that the PWB did not warp symmetrically even though it retained a concave upward shape.

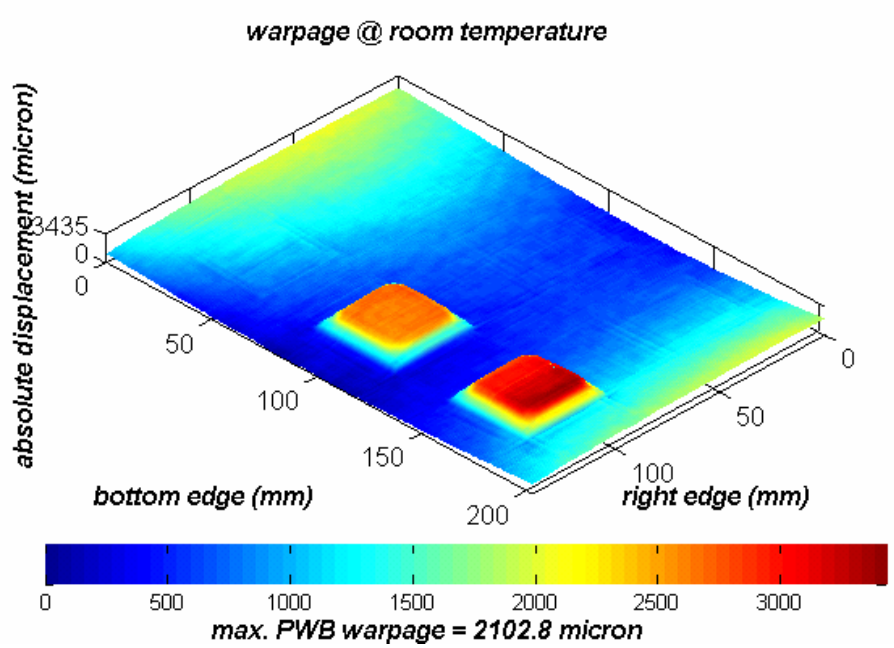


Figure 6.18. Out-of-plane displacement plot of PWBA Configuration 4 at initial room temperature

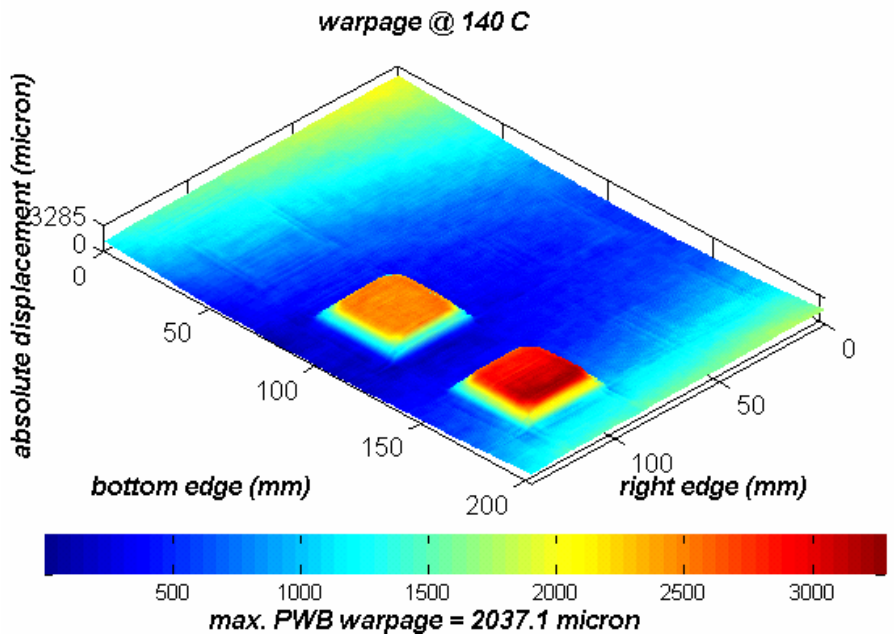


Figure 6.19. Out-of-plane displacement plot of PWBA Configuration 4 at 140 ^{o}C heating

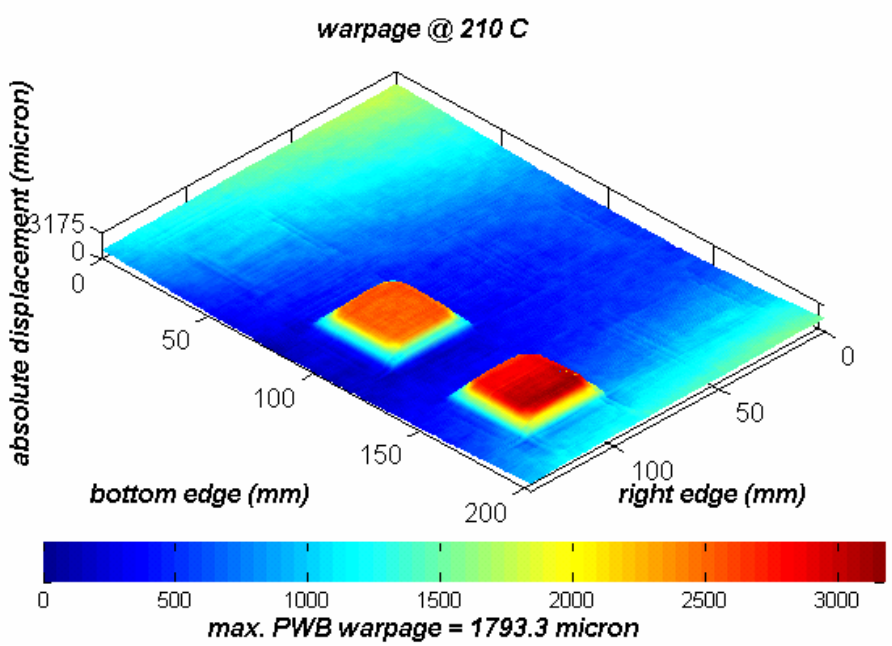


Figure 6.20. Out-of-plane displacement plot of PWBA Configuration 4 at 210 ^{o}C

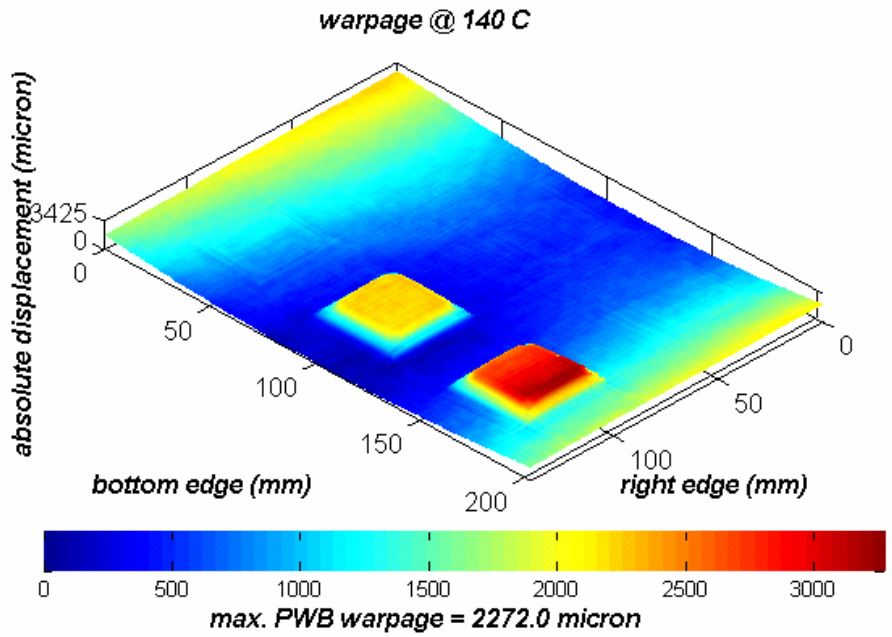


Figure 6.21. Out-of-plane displacement plot of PWBA Configuration 4 at 140 ^{o}C cooling

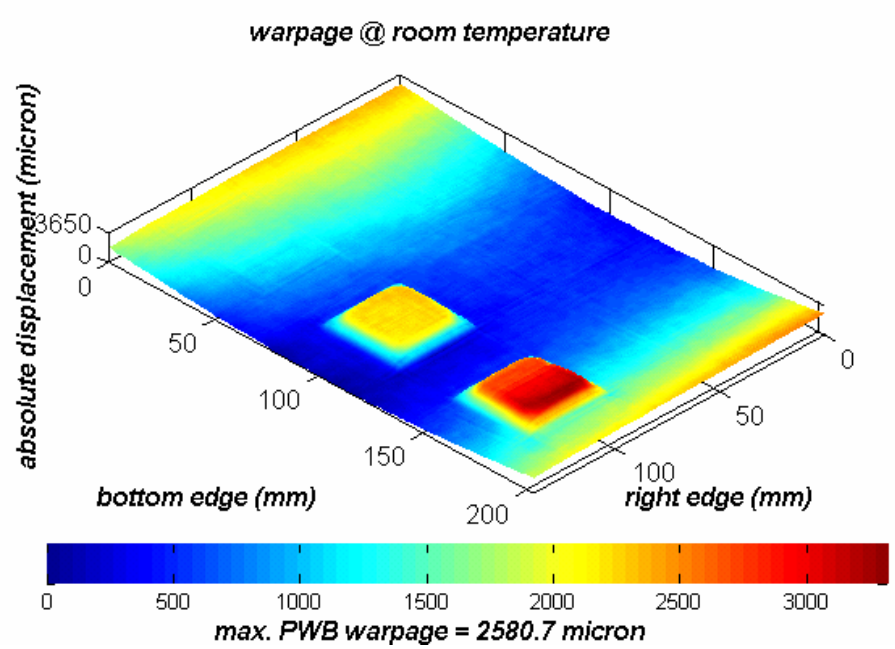


Figure 6.22. Out-of-plane displacement plot of PWBA Configuration 4 at final room temperature

6.4 Discussion of PWBA Test Vehicle Warpage Measurement Results

As shown in the previous section, for every PWBA configuration measured, the PWB warped in a concave upward fashion. From room temperature to the peak temperature of 210 ^{o}C, the maximum warpage of the PWB decreased, and as the assembly was cooled from 210 ^{o}C back to room temperature, the maximum warpage of the PWB increased. Table 6.1 shows the measured maximum warpage results for the four PWBA configurations. For every configuration measured, the maximum warpage of the PWB at room temperature after convective heating exceeded the maximum warpage at room temperature before the convective heating process. The increase in maximum

Table 6.1. Maximum Warpage Results for PWBA configurations

	PWBA Configuration			
Temperature (^{o}C)	**Maximum PWB Warpage of PWBA Configuration 1 (microns)**	**Maximum PWB Warpage of PWBA Configuration 2 (microns)**	**Maximum PWB Warpage of PWBA Configuration 3 (microns)**	**Maximum PWB Warpage of PWBA Configuration 4 (microns)**
25 ^{o}C	2158.9	2256.2	2175.8	2102.8
140 ^{o}C Heating	1513.8	1438.9	1742.0	2037.1
210 ^{o}C	967.5	1289.4	1624.4	1793.3
140 ^{o}C Cooling	1669.3	1885.3	2317.6	2272.0
25 ^{o}C	2292.6	2396.1	2660.3	2580.7

warpage after a thermal process is referred to as residual warpage. For Configuration 1, the residual warpage was 133.7 microns. For Configuration 2, the residual warpage was 139.9 microns. For Configuration 3, the residual warpage was 484.5 microns and for Configuration 4, the residual warpage was 477.9 microns. The residual warpage is due to the accumulation of residual stresses in the PWB during the heating process. Table 6.2

Table 6.2. Maximum warpage change between 25 ^{o}C and 210 ^{o}C for four PWBA configurations

	PWBA Configuration			
Temperatures (^{o}C)	**Maximum PWB Warpage Change of PWBA Configuration 1 (microns)**	**Maximum PWB Warpage Change of PWBA Configuration 2 (microns)**	**Maximum PWB Warpage Change of PWBA Configuration 3 (microns)**	**Maximum PWB Warpage Change of PWBA Configuration 4 (microns)**
25 to 210	- 1191.4	- 966.8	- 551.4	- 309.5

shows the maximum warpage change between 25 ^{o}C and 210 ^{o}C for each of the four configurations. Table 6.2 shows that that as the number of PBGA packages on the PWB increases, the maximum warpage of the PWB decreases. This is due to the constraining effects that the PBGA packages has on the PWB. For the case of the PWB with one PBGA package, PWBA Configuration 2 had higher maximum warpage values than PWBA Configuration 3. The out-of-plane displacement plots presented in the previous section showed that the PWBs warped high at the edges near the supports. Therefore, it makes sense that PWBA Configuration 2 has a higher maximum PWB warpage, because the constraining effects of the PBGA package on the PWB edges are minimal.

The maximum warpage change results in Table 6.2 show that with an increasing number of PBGA packages, the maximum warpage change of these PWB configurations during heating decreases, but Table 6.1 shows that the absolute warpage is greater for PWBAs than for the bare PWB especially at the peak reflow temperature. More studies with other PWB and chip package types are needed to see if this trend is generally true. To study the effects of the PBGA packages on local and global PWB out-of-plane displacements, for each configuration, the out-of-plane displacement at each PWB corner were compared with each other at room temperature after the convective heating process. Table 6.3 shows the out-of-plane displacement values for each PWB corner for the four configurations studied. For PWBA Configuration 1, the only trend that can be observed is that the out-of-plane displacements at the bottom right and left corners of the PWB are larger than the out-of-plane displacements at the top right and left

Table 6.3. Room temperature PWB corner displacements for four configurations

	PWBA Configuration			
PWB Location	**Out-of-Plane Displacements of PWBA Configuration 1 (microns)**	**Out-of-Plane Displacements of PWBA Configuration 2 (microns)**	**Out-of-Plane Displacements of PWBA Configuration 3 (microns)**	**Out-of-Plane Displacements of PWBA Configuration 4 (microns)**
Top Left	1779.8	2331.5	2656.1	2333.1
Top Right	1893.4	2335.4	2495.5	2554.2
Bottom Right	2250.1	2395.7	2129.8	1771.3
Bottom Left	2290.6	2383.2	2542.1	1816.1

corners. Table 6.3 shows the same trend for PWBA Configuration 2 that was observed for Configuration 1. However, for Configuration 2, the bottom PWB corner out-of-plane displacements are only larger than the top out-of-plane displacements by less than 65 microns. For Configuration 1, the bottom PWB corner out-of-plane displacements were larger than the top PWB corner out-of-plane displacements by at least 350 microns. This suggests that the PBGA package has an effect of lowering the out-of-plane displacements of the bottom PWB corners which are closest to it. Configuration 3 shows a trend that is different from Configurations 1 and 2. For PWBA Configuration 3, the highest corner out-of-plane displacement of 2656.1 microns occurred at the top left location of the PWB. The lowest corner out-of-plane displacement of 2129.8 microns occurred at the bottom right of the PWB where the PBGA package is located. The corner out-of-plane displacement results for PWBA Configuration 3 showed that the PWB corner closest to the PBGA package had the lowest out-of-plane displacement. For PWBA Configuration 4, results similar to Configuration 3 were obtained. The lowest PWB corner out-of-displacement was 1771.3 microns and occurred near a PBGA package. All other PWB corners were far from a PBGA package.

From the results presented in this chapter, two conclusions can be drawn. The first conclusion is that for this particular test vehicle, the maximum warpage of the PWB decreased with the addition of PBGA packages. Secondly, PWB corners close to a PBGA package did not deform as much as they would have if there was no PBGA package for these particular configurations. More studies are needed to determine if this generally holds true for other PWBA types. As shown in Figure 6.1, the test vehicle used in this chapter could only accommodate two PBGA packages in two specific locations. To study the effects of varying PBGA package locations on the test vehicle presented in this chapter, a finite element model (FE) is developed. The FE model is discussed in the next chapter.

CHAPTER 7

PWBA FINITE ELEMENT MODEL

The fourth objective of this research is to develop a finite element (FE) model to study the behavior of PWBs with PBGA packages under thermal loading. The model will be used to study the effect of PBGA package locations on PWB warpage. Since the test vehicle used in this research can only accommodate two PBGA packages, a full chip package placement study could not be performed experimentally. The FE model developed in this chapter will enable PWBA configurations to be evaluated that were inhibited by the available test vehicle.

7.1 PWBA Geometry and Meshing

The PWBA geometry consists of a 203.2 mm by 139.7 mm by 0.631 mm PWB and one or two 35 mm PBGA packages. The PWB is a four-layer PWB which means the PWB has four copper layers and three FR-4 layers [18]. Figure 7.1 shows a schematic of the four-layer PWB used in this research along with its thickness dimensions [18]. The PWB was modeled and meshed using the ANSYS shell91 element,

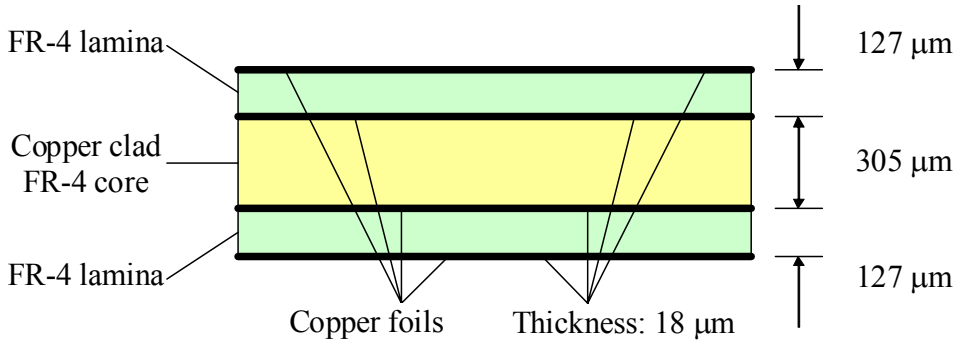


Figure 7.1. Cross-section schematic of test vehicle PWB [18]

which is a nonlinear layered structural shell element. Figure 7.2 shows the shell element that was used for meshing the PWB. Shell elements were used to model the PWB, due to

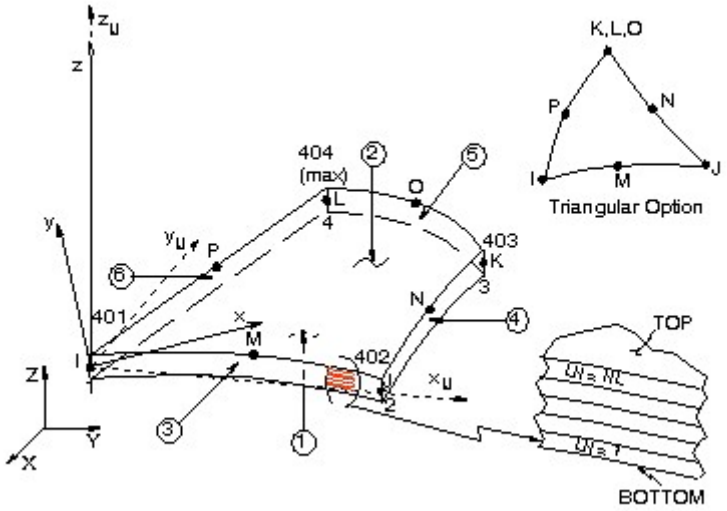


Figure 7.2. ANSYS shell91 element (Taken from ANSYS documentation)

large aspect ratios of the PWBA geometry . For example, the PWB's largest dimension is 203.2 mm, whereas the PWB thickness is only 0.631 mm. If solid elements were used to model the PWB, the node/element limit of the ANSYS package of 128,000 for the research version available on campus would be exceeded. The shell91 element also

provides the advantage of being able to represent the layers of copper and FR-4 in the PWB individually.

The PBGA package modeled in this research has a body size of 35 mm, 352 peripheral solder bumps with a pitch of 1.27 mm. The silicon die is attached to the substrate via wirebonds. Figure 7.3 shows a schematic of a wire bond PBGA chip

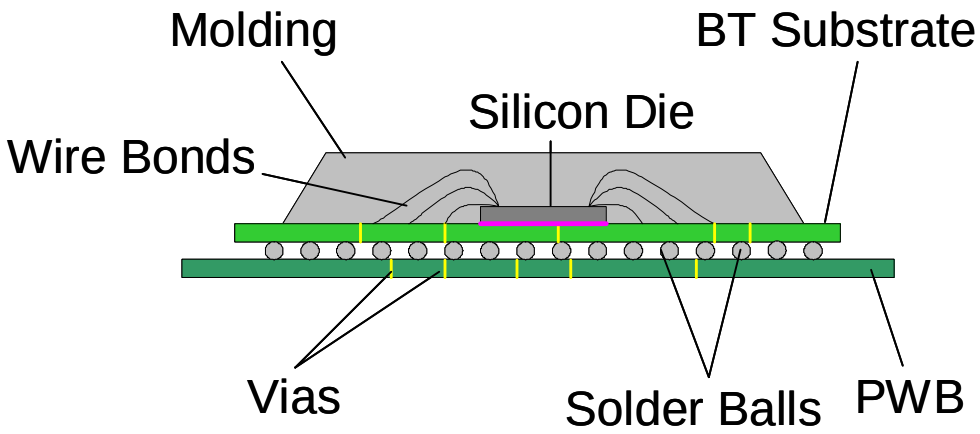


Figure 7.3. Schematic of wire bond PBGA package [18]

package. The silicon die is the brain of the chip package where the computations are performed. Wire bonds are used to connect the silicon die to the bismaleimide triazine (BT) substrate which runs the connection to the solder balls using vias. The solder balls are then connected directly to the PWB. The molding serves to protect the silicon die and to add stiffness to the chip package. All the components of the PBGA package including the silicon die, molding, BT substrate, and solder balls were all modeled using the ANSYS solid95 element. The solid95 element is a 3D 20 node structural solid element which provides the advantage of having mid-side nodes for higher accuracy. The solid element used for modeling the PBGA package(s) is shown in Figure 7.4. For modeling the PBGA packages, the tetrahedral form of the element was used to enable free meshing.

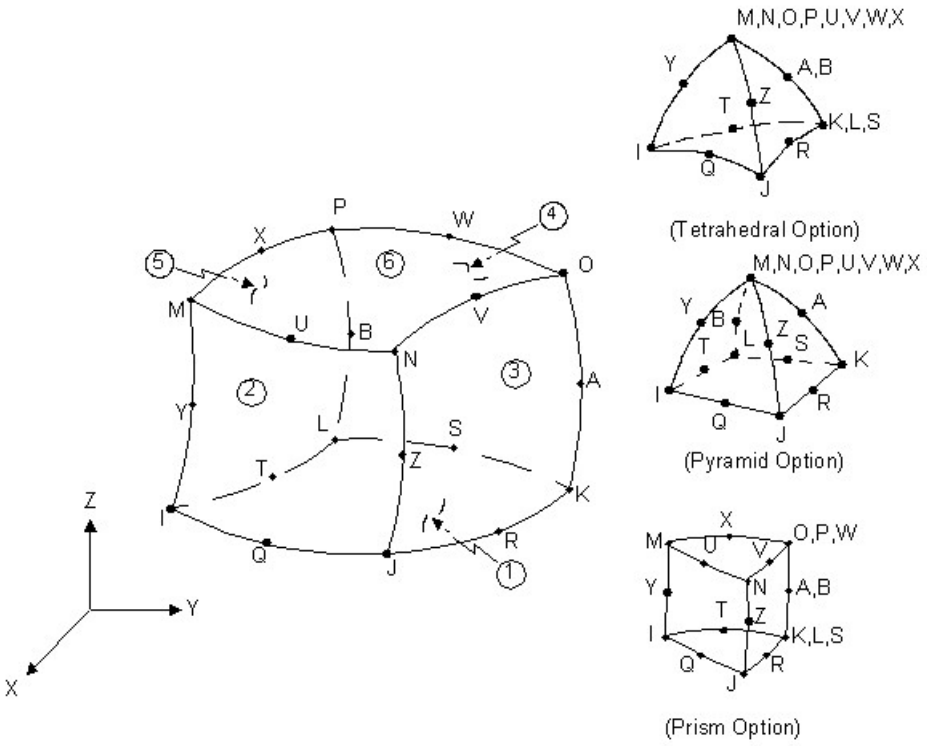


Figure 7.4. ANSYS solid95 element (Taken from ANSYS documentation)

As briefly mentioned in the previous section, the ANSYS version used in this research has a limit of 128,000 nodes or elements. Therefore, in order to study several chip packages on a PWB simultaneously, some model reduction techniques should be used. In this study, the PWBA modeling methodology developed by Ding is used [18]. Using effective modeling, the PBGA package geometry in Figure 7.3 is reduced to the geometry shown in Figure 7.5. In the effective model, the solder bumps are replaced by an equivalent solid layer. The material properties of the equivalent solder layer are determined using simple rule of mixtures.

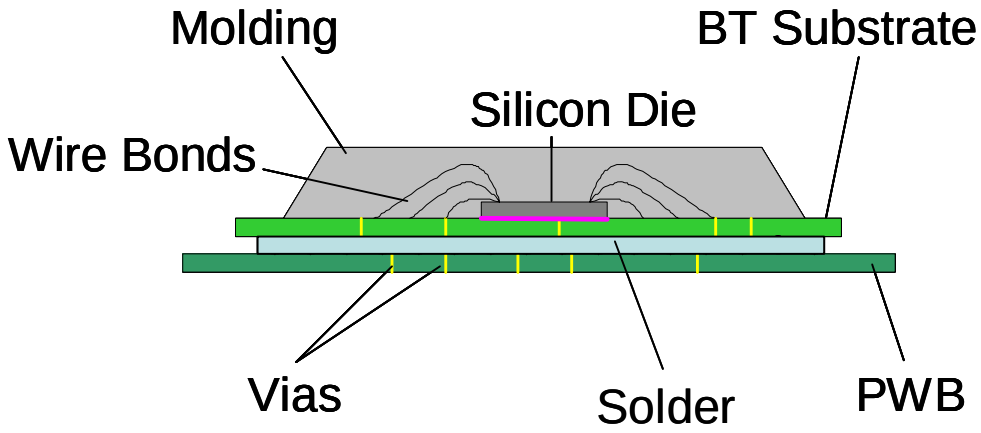


Figure 7.5. Effective modeling of a PBGA package

Figure 7.6 shows the meshed PWB along with a PBGA package modeled using the effective modeling approach.

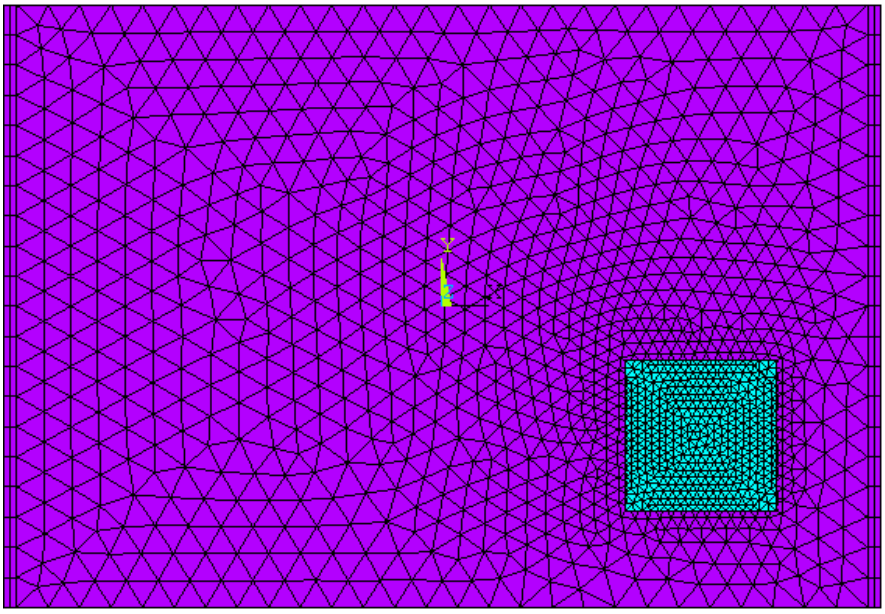


Figure 7.6. Meshed PWB with one PBGA package

To prove that considerable accuracy is not lost by the effective modeling approach, Table 7.1 shows the comparison between maximum PWB warpage results obtained when the PBGA is fully modeled and when the PBGA is modeled using the effective approach.

Table 7.1 shows that the maximum PWB warpage results obtained using effective modeling is only 2.1 % away from the maximum PWB warpage results obtained using

Table 7.1. Maximum warpage results comparison between full and effective modeling of PBGA package

Case	Warpage (microns)	Number of Nodes
Full Model	942.4	98,589
Effective Model	922.8	17.979
Difference	2.1 %	81.8 %

the full model. On the other hand, the number of nodes in the model was reduced by 81.8 %. The results in Table 7.1 show that the effective modeling approach is worthwhile, because the maximum PWB warpage results does not change significantly and the reduction in total number of nodes allows multiple chip packages to be modeled simultaneously. A mesh convergence analysis was also performed on the PWBA. The mesh size was reduced by 25 % and the resulting PWB warpage was 924.0 microns representing a difference of 0.13 % which shows that the mesh is converged.

7.2 Material Properties

The material properties of the materials used in the PWBA model with the exception of FR-4 are shown in Table 7.2. The materials are modeled as linear elastic and isotropic [18] except FR-4 which is modeled as orthotropic and temperature dependent [79]. The material properties of FR-4 are included in Appendix C.

Table 7.2. Material properties used in FE model

Materials	Coefficient of Thermal Expansion, CTE (ppm/K)	Young's Modulus, E (GPa)	Poisson's Ratio, ν
Copper Foil	18.94	79.51	0.32
Sn/Pb Solder	24.7	30.0	0.31
BT Substrate	15	14.0	0.15
PBGA molding	17.5	15.0	0.15
Silicon	2.6	160.0	0.23

7.3 Boundary Constraints and Temperature Loading

In the FE model, the edge nodes of PWB is simply supported along the width directions which is similar to the support condition of the PWBA in the projection moiré warpage measurement system. Note that in the model, the PWB length is in the x-direction, the PWB width is in the y-direction and the PWB thickness is in the z-direction. Therefore, along the width edges of the PWB, the z-displacements are set to equal zero. In addition, to prevent rigid body rotation, the bottom left and right corner nodes are set to have a y-displacement of zero.

The FE model is loaded using a temperature load. The reference temperature is set to be the peak reflow temperature of 210 ^{o}C used in the previous chapter. The reference temperature was set to 210 ^{o}C, because the experiments in Chapter 6 showed that the PWB had the lowest warpage at this temperature. In the FE model, the PWB will have zero warpage at 210 ^{o}C. After setting the reference temperature, the assembly is cooled to room temperature which is assumed to be 25 ^{o}C. The out-of-plane displacement of the PWB is then recorded at room temperature in order to determine maximum PWB warpage.

7.4 FE Model Validation

Before the FE model can be used to study the effect of PBGA package placement locations, it must be validated. To validate the FE model, PWBs with one and two PBGA packages are used. The FE model was temperature loaded from 210 ^{o}C to room temperature and compared with projection moiré experimental results at room temperature. Figure 7.7 and Figure 7.8 show the out-of-plane displacement plots of the PWB with one PBGA package for the FE model and projection moiré experiment respectively. Both Figure 7.7 and Figure 7.8 show that the PWB warped in a concave upward shape. The maximum PWB warpage change from 210 ^{o}C to 25 ^{o}C obtained for the FE model was 922.8 microns. For the projection moiré experiment, the maximum

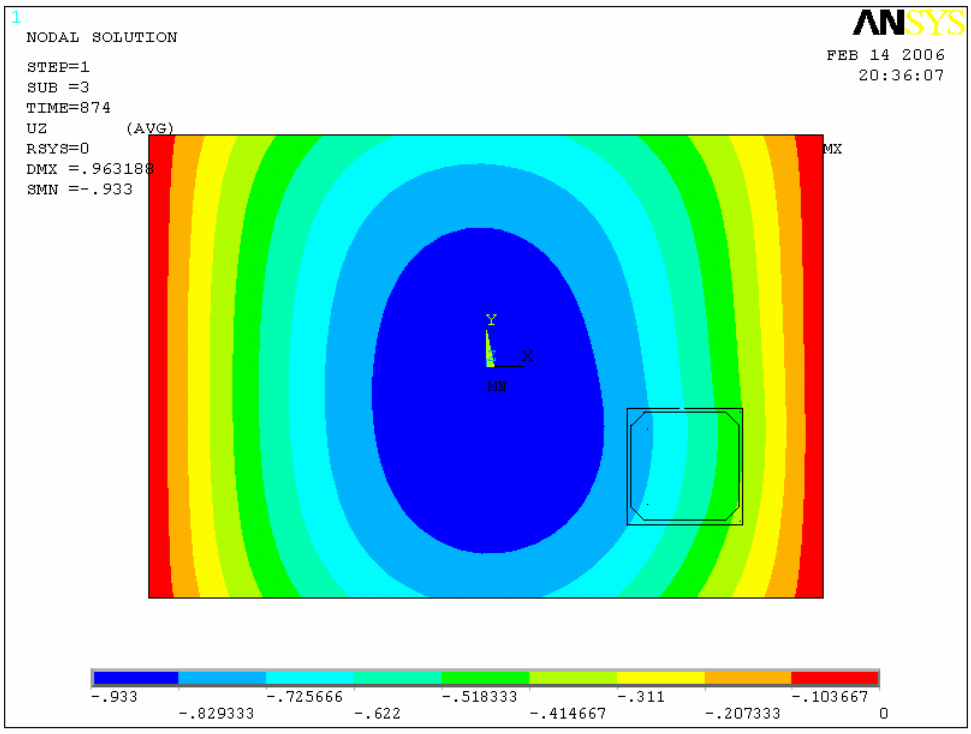


Figure 7.7. FE Out-of-displacement plot of PWB with two PBGA packages at 140 ^{o}C

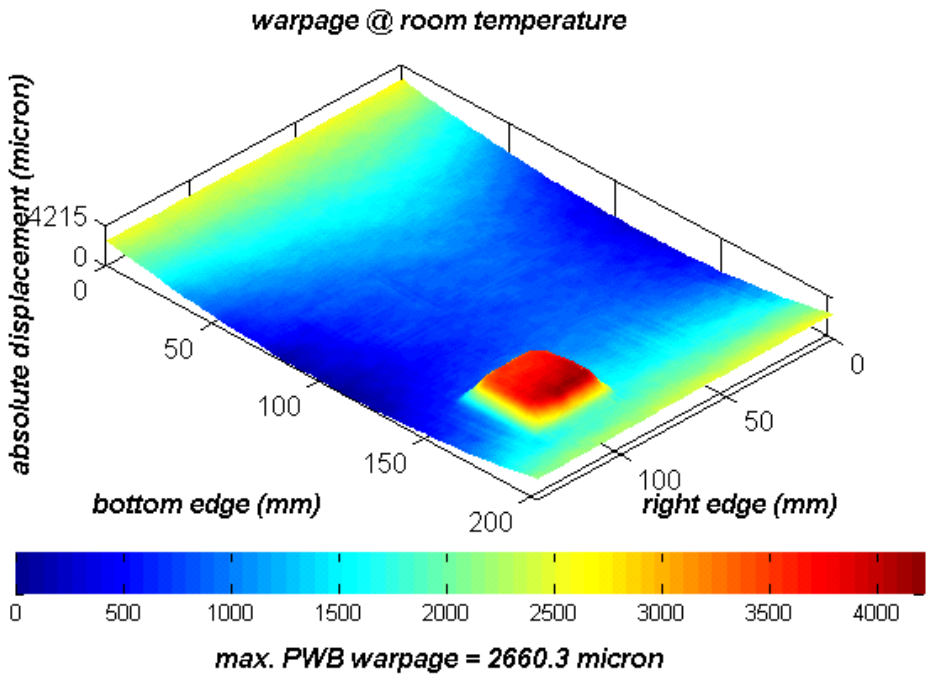


Figure 7.8. Projection moiré out-of-displacement plot of PWB with two PBGA packages at 140 ^{o}C

PWB warpage change from 210 ^{o}C to 25 ^{o}C was 1035.9 microns which is a difference of 10.9 %. Note that in the FE model, the maximum PWB warpage at 210 ^{o}C is zero, whereas for the projection moiré experiment, the maximum PWB warpage at 210 ^{o}C was 1624.4 microns. For the case with two PBGA packages, the maximum PWB warpage obtained from the FE model at room temperature after cooling was 698.7 microns, and the maximum PWB warpage obtained from the projection moiré experiment at room temperature was 787.4 microns which is a difference of 11.3 %. The FE model and projection moiré experimental results show that the model results agree well with experimental results.

The difference between the modeling and experimental results can be due to a number of reasons. First, temperature dependent material properties for FR4 are very hard to find in the literature. Even if FR4 material properties are found, the chance of

those material properties being equal to the material properties of the FR4 in the PWB being modeled is very slim. There are many manufactured variations of FR4 and many manufacturers are sometimes hesistant to reveal the exact material buildup. The FR4 material properties used in this research was for FR4 having a laminate construction of 60 fibers/inch in the warp direction and 58 fibers/inch in the fill direction. The FR4 in the PWB being modeled in this research has a laminate construction of 60 fibers/inch in the warp direction and 47 fibers/inch in the fill direction. The discrepancy between the fiber counts in the fill direction is one possible cause of the maximum PWB warpage difference between FE modeling and experimental results. Another possible cause of the maximum PWB warpage difference between the FE modeling and experimental results could be the support conditions in the model. When warpage experiments are conducted using the projection moiré system, the PWB/PWBA is supported on invar rails typically on the short edges of the PWB/PWBA. To simulate the real world support conditions, the entire short edges of the PWB/PWBA were set to have zero out-of-plane displacements. Although this closely simulates the experimental support conditions, there is a slight difference, because a real PWB/PWBA can have varying out-of-plane displacements on the support edges. Another possible cause of the maximum PWB warpage difference between FE modeling and experimental results could be due to the fact that the PWB traces were not modeled even though it is highly unlikely. It would be impossible to model the traces with the node/element limit of the academic version of ANSYS, since the traces are much smaller than the rest of the model. Even though the FE model and projection moiré experiments doesn't match exactly, it can still be used to perform

PWBA warpage studies. In this case, the FE mdoel will be used to perform a chip package placement study for a PWB with one, two and three PBGA packages.

7.5 PBGA Package Layout Study

In this section, the developed FE model is used to study the effect of the layout of PBGA packages on PWB warpage during thermal loading such as cooldown after reflow. The results can be used as layout guidelines for PWB layout designers who may have choices of PBGA package design locations. In this section, the warpage of the PWB is studied with one, two and three PBGA packages. The locations of the PWB that will studied were determined by dividing the PWB into three segments in the length and width directions to create a total of nine locations. A 3 by 3 matrix of locations were chosen, because it is the smallest dimension that would allow a chip package to be placed in the center of the PWB as well as fit in the divided segment. For the one PBGA package case, the layout configurations that were studied are shown in Figure 7.9. The number 1 is used to represent the PBGA package. Note that for each segment used, the PBGA package is placed at the center.

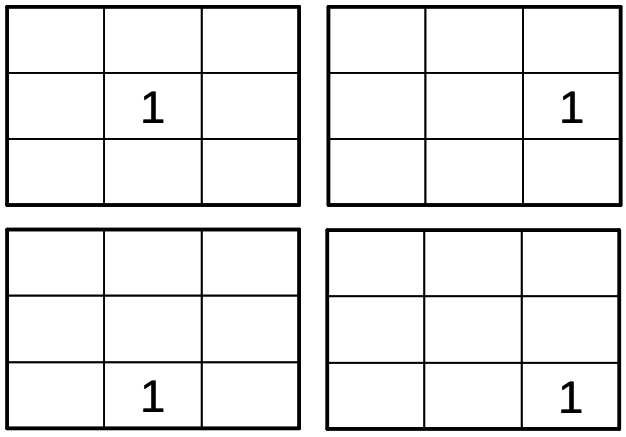


Figure 7.9. PWBA layout configurations for one PBGA package

Since the PWB is supported symmetrically, only four PWB locations need to be studied for the one PBGA package case. Similar to the previous cases discussed in this thesis, the PWBA was temperature loaded from 210 ^{o}C to 25 ^{o}C. The PWBA configuration that had the highest maximum PWB warpage was the case with the PBGA package in the center of the PWB as shown in Figure 7.10. The PWB warpage obtained in Figure 7.10 was 968.3 microns. The configuration that had the next highest maximum PWB warpage was the configuration with the PBGA package at the middle of the long edge of the PWB. The warpage of this configuration was 929.4 microns and is shown in Figure 7.11. The PWBA configuration that had the lowest maximum PWB warpage was the configuration

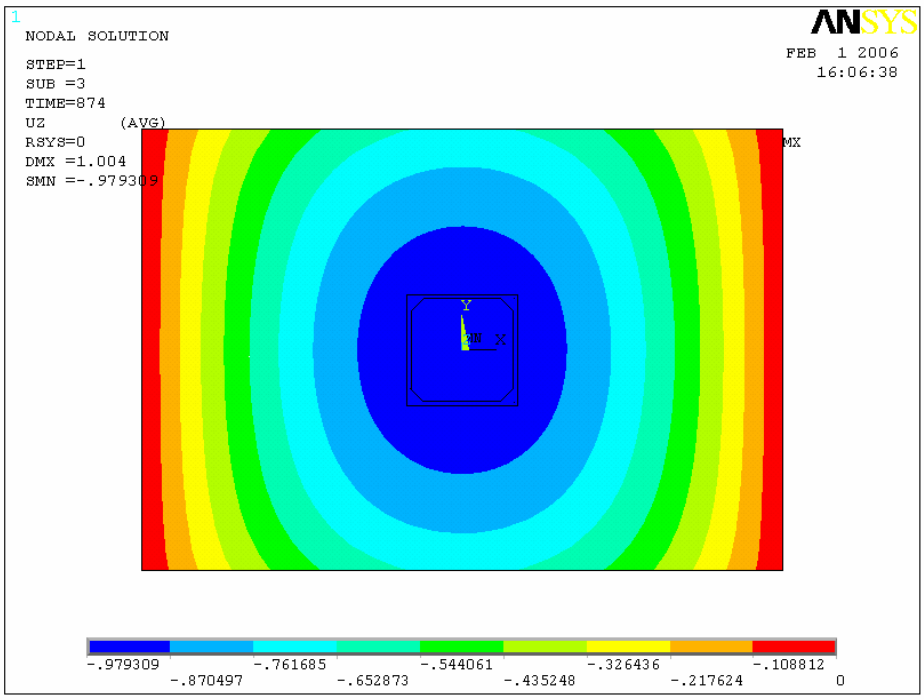


Figure 7.10. PWBA with one chip package configuration having highest maximum PWB warpage

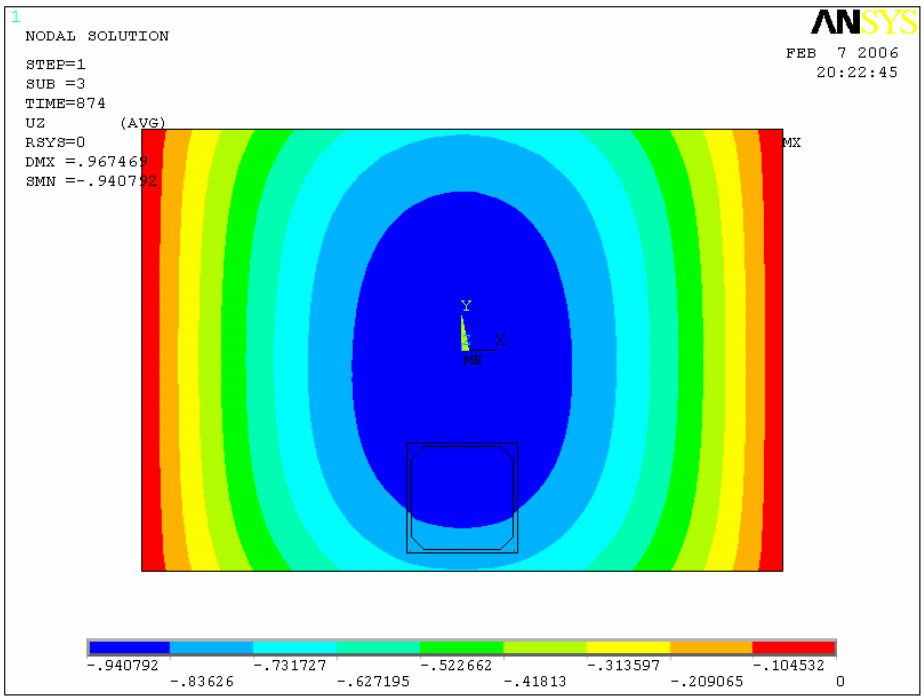


Figure 7.11. PWBA with one chip package configuration having second highest maximum PWB warpage

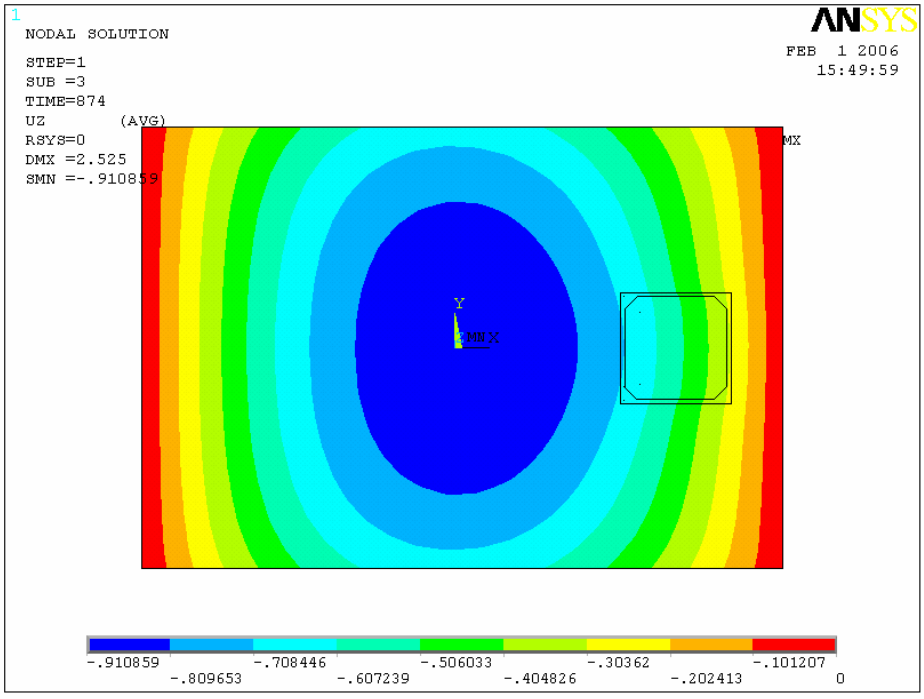


Figure 7.12. PWBA with one chip package configuration having lowest maximum PWB warpage

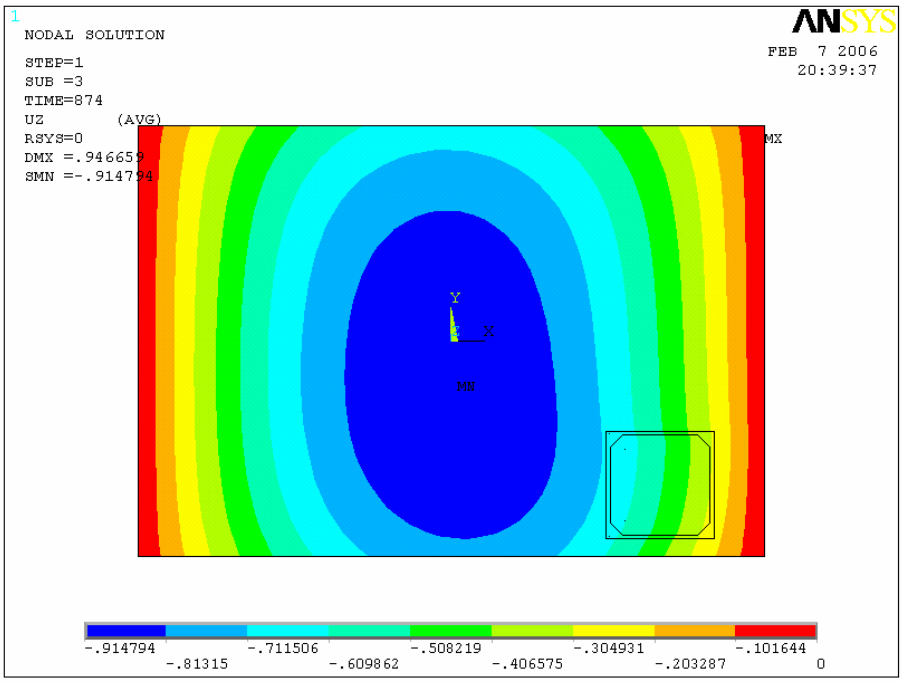


Figure 7.13. PWBA with one chip package configuration having second lowest maximum PWB warpage

with the PBGA package at the middle of the short edge of the PWB as shown in Figure 7.12. The PWB warpage obtained in Figure 7.12 was 899.9 microns. The PWBA configuration that had the next lowest maximum PWB warpage was the configuration with the PBGA package at the corner of the PWB. The warpage of this configuration was 904.5 microns and is shown in Figure 7.13. The results for the PWBA configurations with one PBGA package showed that the PBGA package locations near the support edges of the PWB resulted in lower warpage when compared to the PBGA package locations further away from the PWB support edges. The PWB support edges were further away from the PWB center than the PWB edges that were not supported. For the two PBGA package locations near the support edges of the PWB, the PWB warpage did not change much and was much lower than the cases located away from the PWB support edges.

For the two PBGA package case, the layout configurations that were studied are shown in Figure 7.14 and Figure 7.15. Once again, numbers are used to represent the PBGA packages. Due to symmetry, only 13 PBGA package locations are studied. For the PWBA with two chip packages, the configuration that had the highest

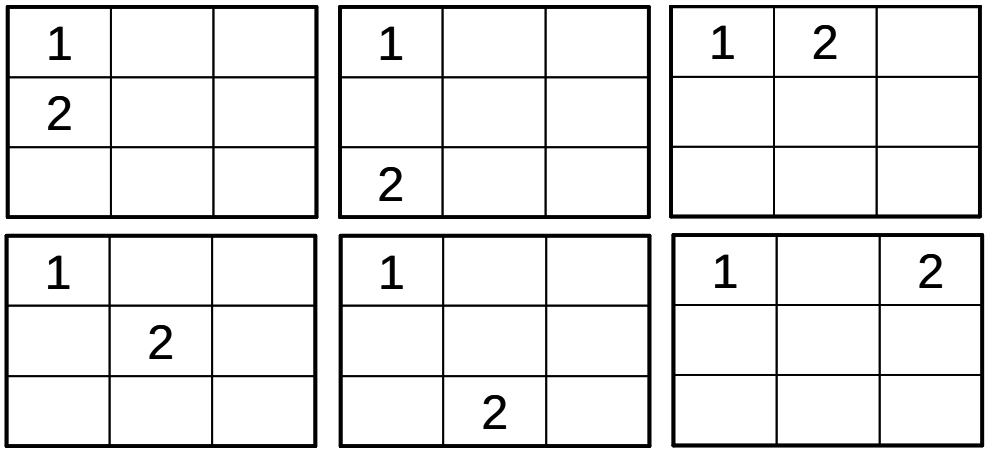


Figure 7.14. First six PWBA layout configurations for two PBGA packages

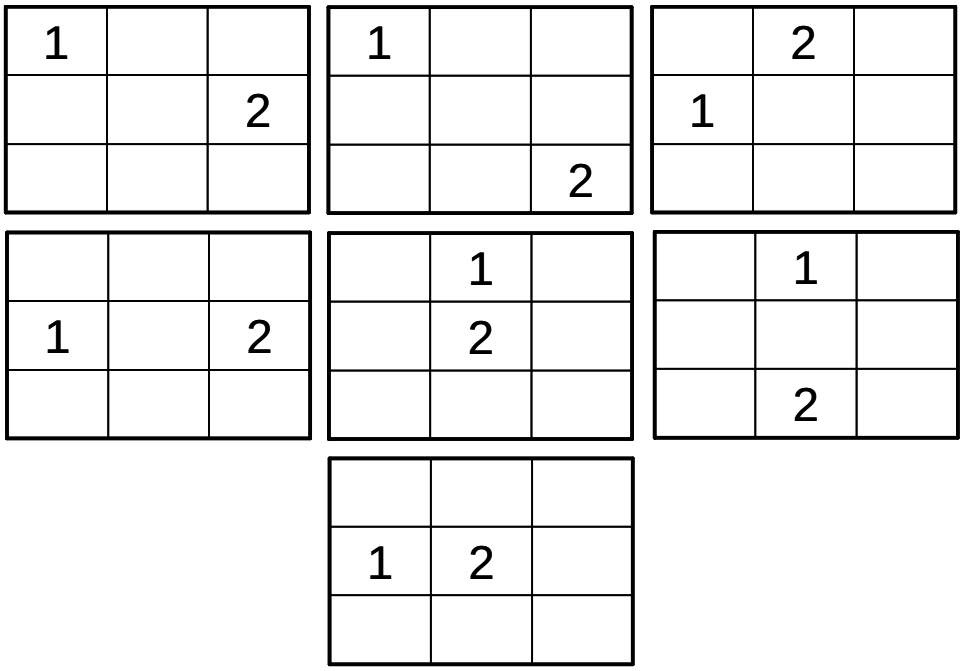


Figure 7.15. Final seven PWBA layout configurations for two PBGA packages

maximum PWB warpage was the configuration with one PBGA package in the center of the PWB and one PBGA package at the center of the long edge of the PWB as shown in Figure 7.16. The PWB warpage obtained in Figure 7.16 was 750.2

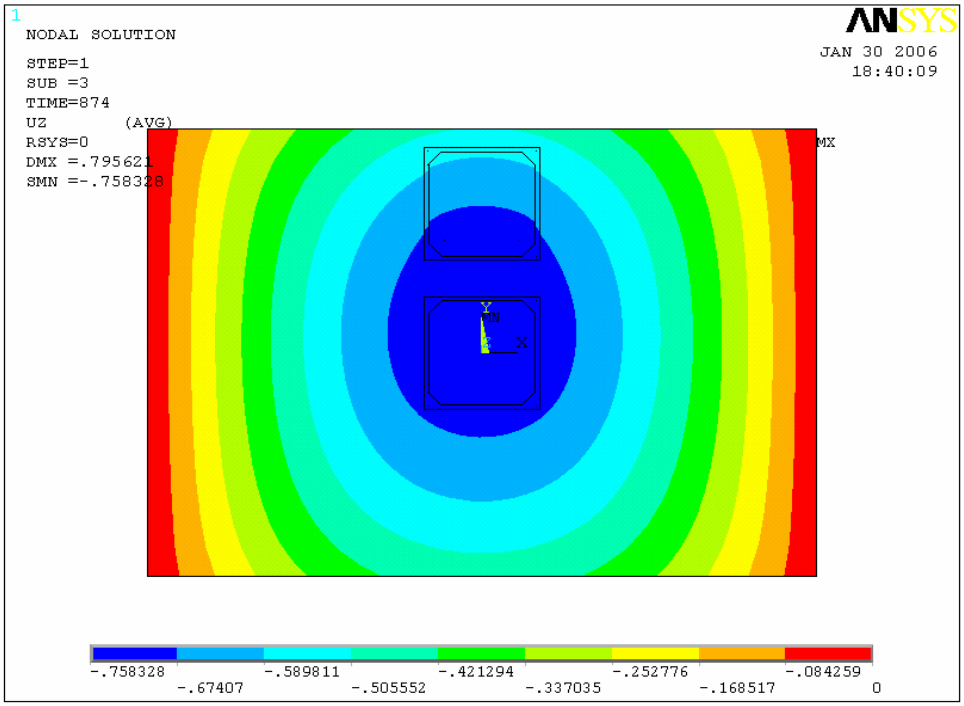


Figure 7.16. PWBA with two chip package configuration having highest maximum PWB warpage

microns. The configuration that had the next highest maximum PWB warpage was the configuration with one PBGA package in the center of the PWB and one PBGA package at the center of the short edge of the PWB as shown in Figure 7.17. The warpage of this configuration was 738.7 microns.

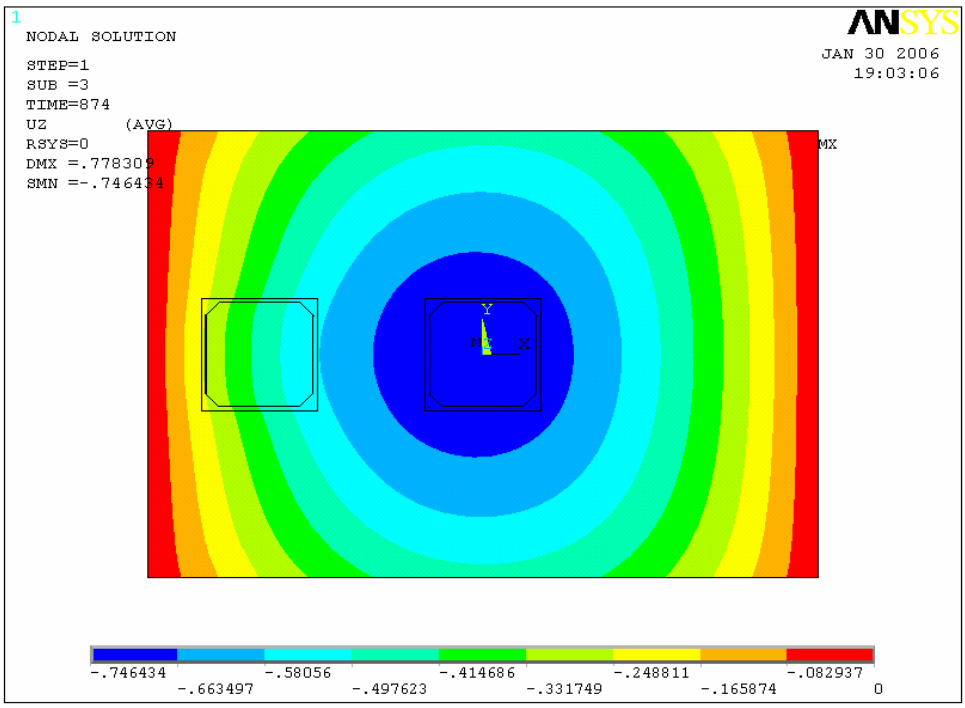


Figure 7.17. PWBA with two chip package configuration having second highest maximum PWB warpage

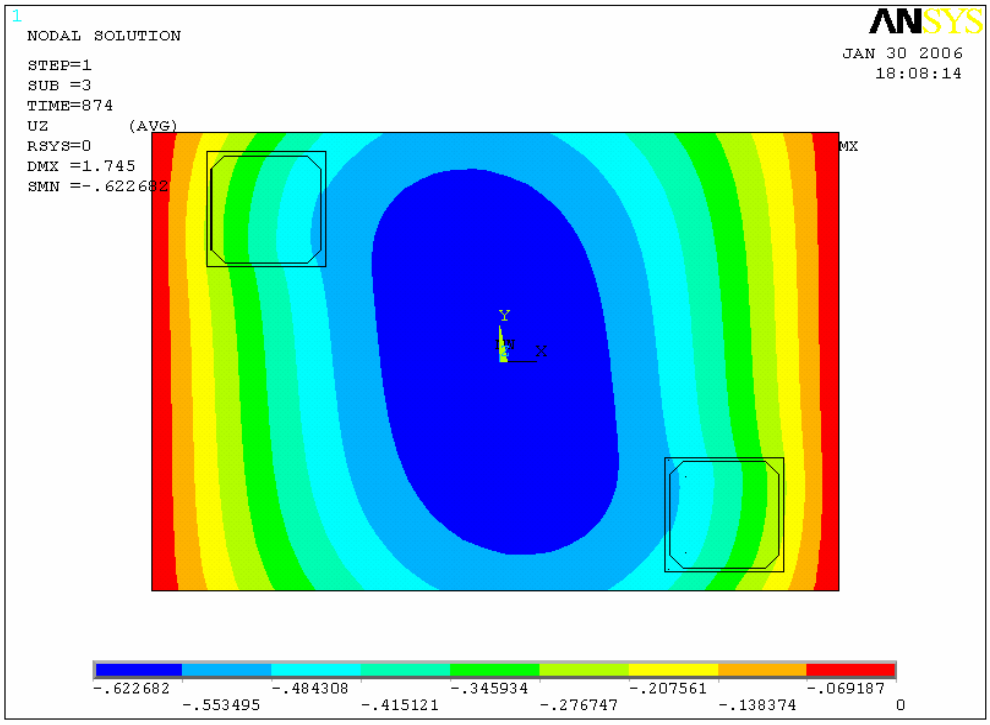


Figure 7.18. PWBA with two chip package configuration having lowest maximum PWB warpage

For the PWBA with two chip packages, the configuration that had the lowest maximum PWB warpage was the configuration with one PBGA package at one corner of the PWB and the other PBGA package at the opposite corner of the PWB as shown in Figure 7.18. The PWB warpage obtained in Figure 7.18 was 615.3 microns. The PWBA configuration that had the next lowest maximum PWB warpage was the configuration with one PBGA package in the center of the PWB short edge and the other PBGA package at one of the opposing corners as shown in Figure 7.19. The warpage of this configuration was 622.2 microns. The FE layout results for the PWBA

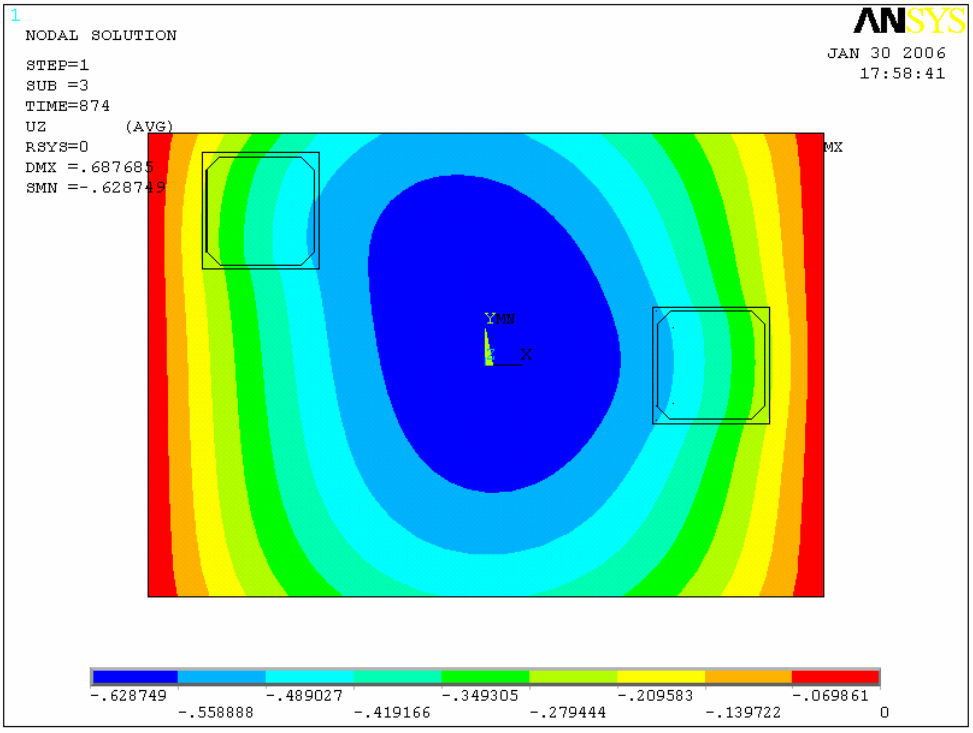


Figure 7.19. PWBA with two chip package configuration having second lowest maximum PWB warpage

with two PBGA packages show that in order to obtain a low warpage due to PBGA package layout, the PBGA packages must be placed on opposing sides of the PWB. Also,

both PBGA packages should be placed near the edges of the PWB furthest away from the PWB center to obtain a low warpage result.

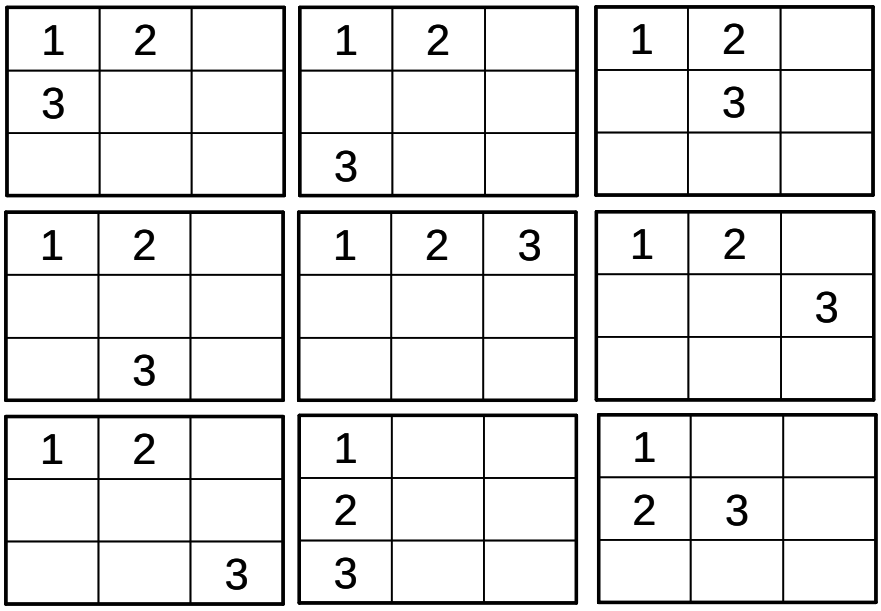


Figure 7.20. First nine PWBA layout configurations for three PBGA packages

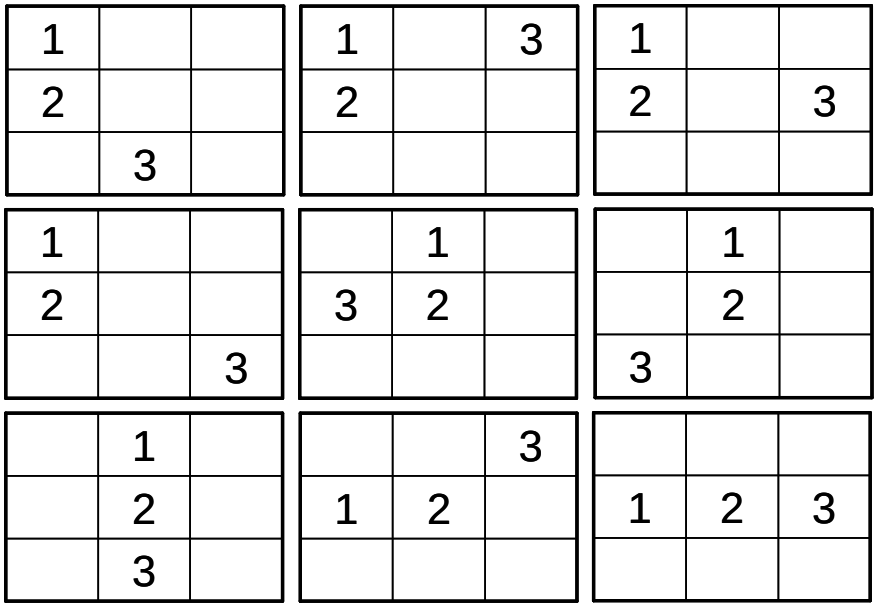


Figure 7.21. Second nine PWBA layout configurations for three PBGA packages

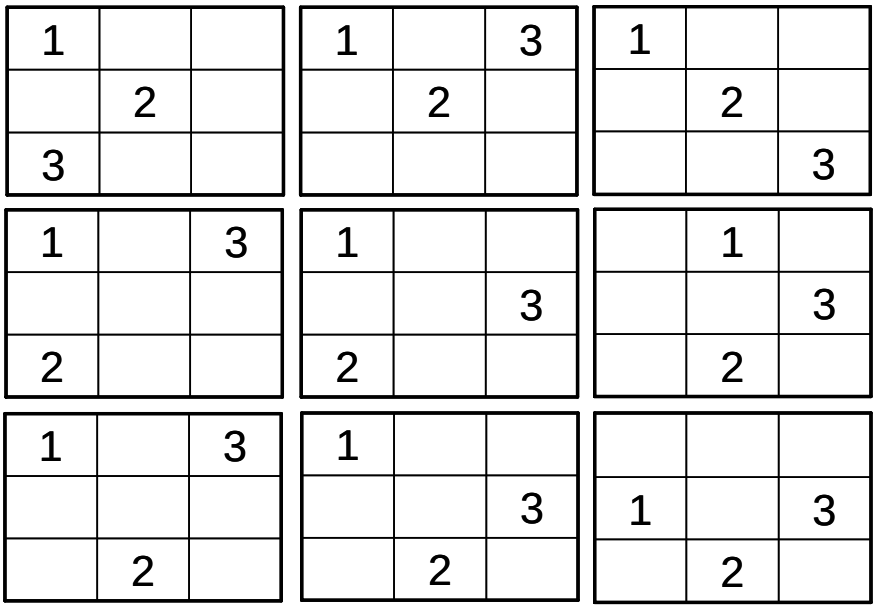


Figure 7.22. Final nine PWBA layout configurations for three PBGA packages

For the three PBGA package case, the layout configurations that were studied are shown in Figure 7.20 to Figure 7.22. Once again, numbers are used to represent the PBGA packages. For the PWBA with three chip packages, the configuration that had the highest maximum PWB warpage was the configuration with all three PBGA packages along the centerline of the PWB in the width direction as shown in Figure 7.23. The PWB warpage obtained in Figure 7.23 was 608.7 microns. The PWBA configuration that had the next highest maximum PWB warpage was the configuration with two PBGA packages lined up along the centerline as in the previous case and the third PBGA package located at the center of the short PWB edge. This configuration has a maximum PWB warpage of 608.2 microns and is shown in Figure 7.24.

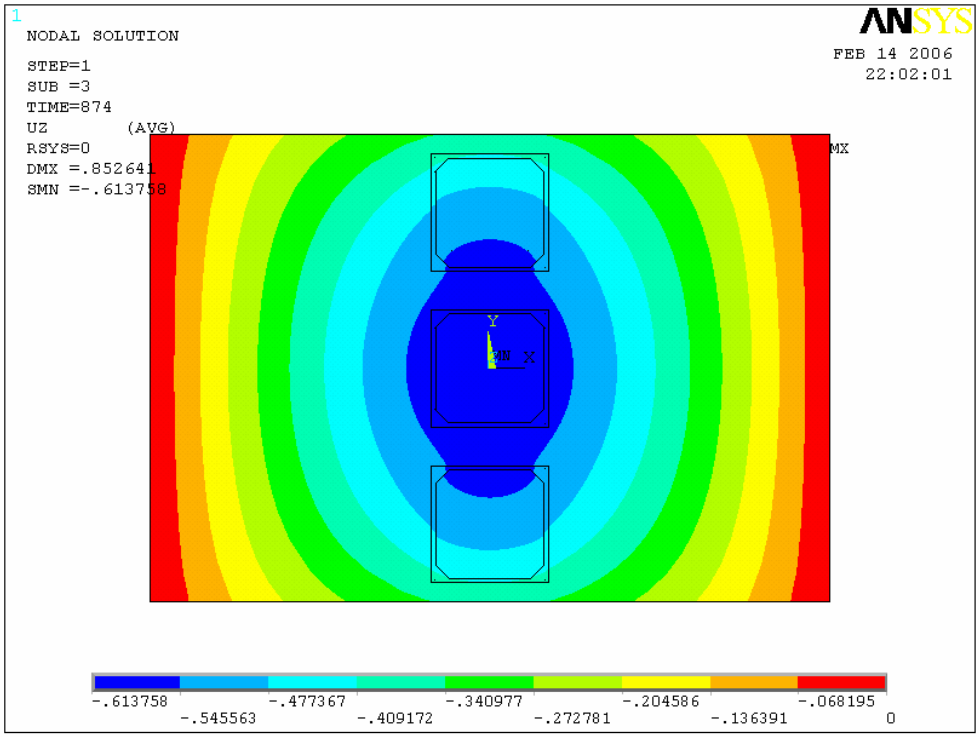


Figure 7.23. PWBA with three chip package configuration having highest maximum PWB warpage

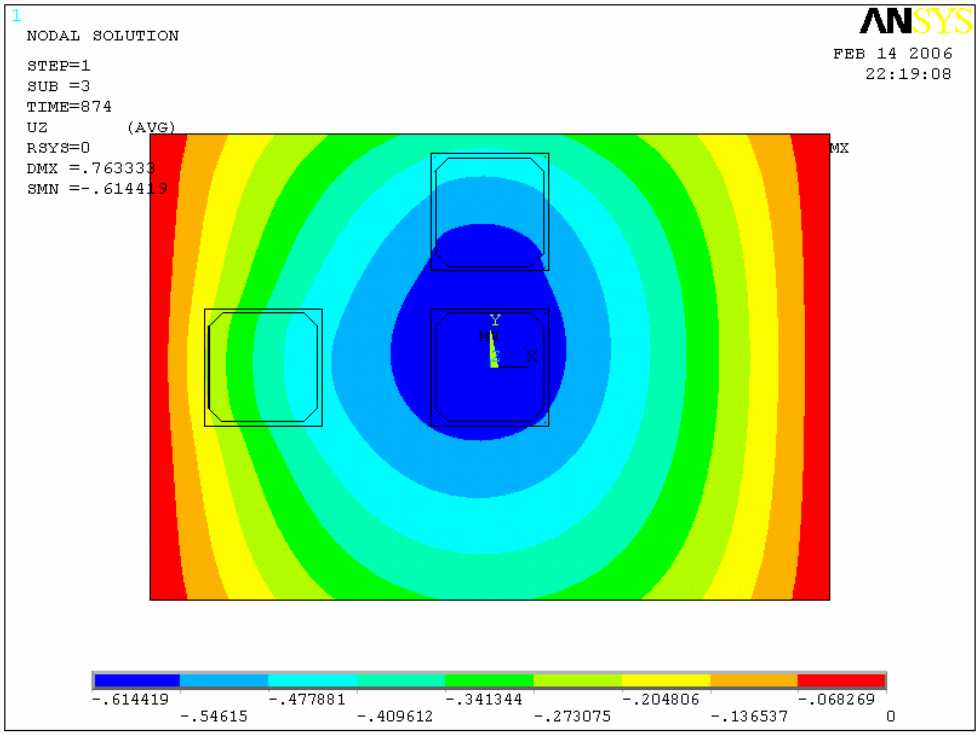


Figure 7.24. PWBA with three chip package configuration having second highest maximum PWB warpage

For the PWBA with three chip packages, the configuration that had the lowest maximum PWB warpage was the configuration shown in Figure 7.25. The configuration shown in Figure 7.25 had a maximum PWB warpage of 424.4 microns. The PWBA configuration that had the next lowest maximum PWB warpage was the configuration shown in Figure 7.26. The PWBA configuration shown in Figure 7.26 had a maximum PWB warpage of 424.0 microns.

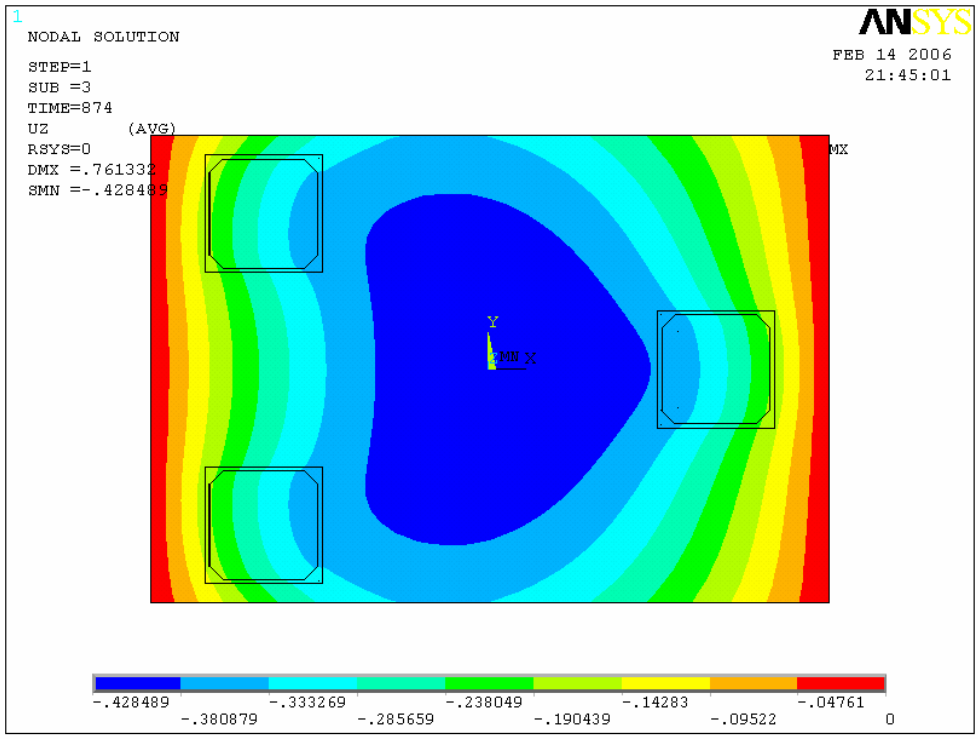


Figure 7.25. PWBA with three chip package configuration having lowest maximum PWB warpage

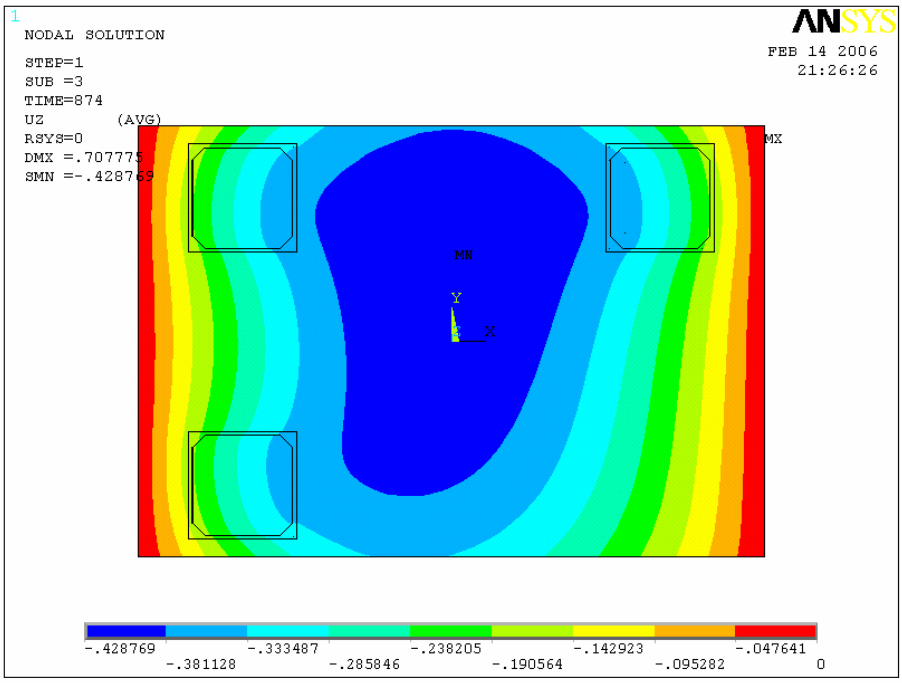


Figure 7.26. PWBA with three chip package configuration having second lowest maximum PWB warpage

The maximum warpage results for the PWBA with three chip packages show that to minimize maximum PWB warpage, the PBGA packages should be placed along the edges of the PWB furthest away from the PWB center. In addition, all three chip packages should not be placed on the same side of the PWB and for the two that are placed together, they should be as far apart as possible.

The FE results with the PWB populated with one, two or three PBGA packages all show that maximum PWB warpage occurred with the chip packages placed near the PWB edges of the PWB furthest away from the PWB center. For the two PBGA package case, the PBGA packages were placed as far apart as possible for minimum warpage. For the three PBGA package, the minimum warpage configuration occurred with two chip packages on one side of the PWB and the third on the other side of the PWB. The third PBGA package was located such that it was equal distances from the other two PBGA

packages. The results presented in this chapter may be useful for PWB layout designers. Although PWB layout designers may have layout restrictions for electronic components, if multiple choices are available, a layout based on the above recommendation may be used as guides to minimize PWB warpage during the assembly process. Further studies are needed to determine if these observations will hold for other PWBA configurations.

CHAPTER 8

CONCLUSIONS

This chapter concludes this thesis work. First, the research objectives, approach and results of each research area are summarized. Next, the major contributions of the research are presented. Finally, recommendations for future work are provided.

8.1 Conclusions

PWB/PWBA/chip package warpage is a common thermomechanical reliability concern in electronic packaging. The overall objective of this research was to develop a warpage measurement system capable of measuring PWBs populated with chip packages during convective heating processes and to utilize the developed system along with finite element modeling to perform a warpage study. The first objective of this research was to design and implement a forced convective heating system for use with the current warpage measurement system. Forced convective heating enables the accurate simulation of forced convection reflow. In previous warpage measurement research performed in the Advanced Electronic Packaging Laboratory (AEPL), infrared heating was used to heat the warpage measurement samples. Infrared heating induces a very large temperature difference through the thickness of the PWB which will affect the warpage measurement results. Before this research was undertaken, the oven was capable of convective heating. The previous design had a few problems. The 3,750 W heater in the oven was not powerful enough, the airflow design did not allow sufficient air to flow over the heater

and the fan was mounted directly on to the oven inducing severe vibrations that affected the warpage measurement. Also, the air velocity could not be varied due to only one speed setting of the fan. The PWB heating rate that resulted from the previous system was a mere 0.02 ^{o}C/second which is 100 times lower than the 2 ^{o}C/second needed to simulate a typical ramp to dwell, ramp to peak reflow (RDRP) profile. The goal of the convective heating system designed in this research was to overcome the drawbacks of the previous convective heating system and to enable the system to simulate industry reflow profiles such as the RDRP profile and the Lee optimized profile. The convective heating system designed in this research uses 12 tubular heaters totaling 36 kW, a large centrifugal fan mounted outside the oven and all supporting ductwork. To eliminate the transfer of vibration from the fan to the oven, the fan was connected to the oven using a flexible connector duct. Also, the fan was mounted on vibration isolators for added protection. The ductwork was designed to incorporate air dampers such that one setting is used for the recirculation of air and the other setting is used for oven cooling by drawing in fresh air and expelling hot air. The PWB heating rate results obtained using the designed convective heating system showed that the maximum heating rate is 0.6 ^{o}C/second, which is a significant increase over the previous convective heating system. The heating rate results also showed that convective heating significantly reduces the through-the-thickness temperature difference when compared to infrared heating. The designed system as a result of this research can be used to simulate Lee optimized reflow profiles. In order to enable the convective heating system to simulate profiles such as the RDRP profile, a CFD model of the system was developed in FLUENT. The CFD model ws used to study critical oven parameters such as heater power, heater surface area and

system volume. The three parameters were studied using a 3 factor, 2 level, full-factorial design of simulations (DOS) and regression. The results of the DOS showed that heater power was the most influential parameter followed by heater surface area and system volume. The results of the regression showed that in order to enable the convective system to heat PWBs at a rate of 2 ^{o}C/second, all three of the studied parameters must be changed. An example of suitable parameter settings would be a heater power of 68 kW, a heater surface area of 2.32 m^2 and a system volume of 0.33 m^3.

The second objective of this research was to improve the software based digital image processing capability of the projection moiré warpage measurement system to enable automated PWBA measurements. The previous projection moiré system utilized at the Georgia Tech AEPL was capable of capturing an image of PWB warpage. The system software for calculating the maximum warpage across the surface of the PWB was designed for bare PWBs. The warpage across the surface of a bare PWB is the difference between the maximum PWB out-of-plane displacement and the minimum PWB out-of-plane displacement. When chip packages are present, the system software calculates an incorrect maximum warpage across the PWB surface, because the maximum PWB out-of-plane displacement will be at the top of the tallest component on the PWB. To overcome the problem of calculating an incorrect maximum warpage result using the projection moiré system when chip packages are present, chip package segmentation method was needed. Several methods were considered including a manual segmentation technique, thresholding and edge based techniques. The major shortcomings of the manual segmentation method were that a mask file would have to be created for each warpage measurement point for a particular PWBA sample. Also, the

experimenter would need to know the exact chip package locations a priori. Therefore, the manual segmentation method was not chosen. Automatic segmentation techniques were explored next. An automatic segmentation technique such as thresholding was not chosen, because the correct segmentation threshold would vary depending on the PWBA sample. The algorithm that was developed for chip package segmentation was an edge-based technique that incorporated the use of active contours (snakes). The algorithm involved five major steps. The first step was to find the edges in the out-of-plane displacement image using the Canny edge detector. The second step was to subsample the 480 pixel by 512 pixel Canny edge image to obtain a 60 pixel by 64 pixel image. The third step involved searching the subampled image using an automatic search method developed in this thesis to locate the approximate location of the chip packages so that initial snakes can be drawn. After the initial snake is drawn, in the fourth step, the Greedy algorithm is used to converge the initial snake onto the chip package edges. The fifth and final step of the algorithm was to use the coordinates of the converged snake points to determine the locations of the PWBA that should be omitted when calculating PWB warpage. Subsequently, the omitted locations are used to determine chip package warpage. The research results showed that the optimal search neighborhood for the Greedy algorithm was a 5 pixel by 5 pixel neighborhood and that initial snake size is much more important than the number of snake points. In addition to developing an automatic chip package detection algorithm for the projection moiré system, a repeatability study on the projection moiré system was performed. The experimental results showed that the projection moiré system has a repeatability of 0.9 % which is excellent.

The third objective of this research was to utilize the convective reflow projection moiré system to study the warpage of PWBA test vehicles. The PWBA test vehicle that was studied was a 203.2 mm by 139.7 mm by 0.631 mm PWB populated with one or two 35 mm, 352 bump peripheral array PBGAs. The goal of the study was to determine the effect of PBGA packages on PWB warpage. The convective heating system was used to heat the PWBA from room temperature to a peak of 210 ^{o}C and then to cool the PWBA back to room temperature. The projection moiré technique was used to measure the warpage of the PWBA at initial room temperature, 140 ^{o}C heating, 210 ^{o}C, 140 ^{o}C cooling and final room temperature. Four configurations of the PWBA were measured: the PWB with no PBGA packages, the PWB with one PBGA package in the middle of the PWB, the PWB with one PBGA package at the PWB edge and the the PWB with two PBGA packages. The experimental results showed that PWB warpage decreased with increasing number of PBGA packages. Also, out-of-plane displacement plots of the PWBA showed that chip packages had minimal effects on PWB edges far away from the chip package according to Saint Venant's principle. The corner of the PWB closest to the PBGA package(s) had the lowest displacement when compared to the other PWB corners.

The fourth and final objective of this research was to develop an FE technique that can be used to study the effects of PBGA package locations on PWB warpage. The FE model was specifically developed to study PBGA locations not allowed using the available test vehicle. In order to use ANSYS to study a PWBA with more than one PBGA package, some geometry simplifications must be made due to the maximum number of nodes available in the academic version of ANSYS. The FE results showed

there is no significant loss in model accuracy if the PBGA package solder bumps are replaced by a uniform solder layer whose effective properties are determined using micromechanics. The FE model was validated using projection moiré experiments and used to study the warpage of a PWB with one, two and three PBGA packages respectively. In every case studied, the minimum warpage occurred when the PBGA packages were placed close to PWB edges far away from the PWB center. More studies are needed on other types of PWBAs to see if these observations generally hold true. These results may be useful for PWB layout designers. Although PWB layout designers may have layout restrictions for electronic components, if multiple choices are available, a layout based on the above recommendation may be used as guides to minimize PWB warpage during the assembly process. Further studies are needed to determine if these observations will hold for other PWBA configurations.

8.2 Summary of Contributions

In this research, a warpage measurement system capable of measuring the warpage of PWBs and chip packages of a PWBA simultaneously during convective heating processes was developed. This is the first available warpage measurement system of its kind. The developed system was used along with a FE model to study the warpage of a PWB with PBGA package(s). The detailed research contributions are listed below.

1. A convective heating system was designed and implemented to be used with the shadow/projection moiré warpage measurement techniques. The implemented system is superior to the previously unusable convective heating system. The convective heating system can be used to simulate convective

reflow for profiles with a ramp rate of less than 0.6 ^{o}C/second such as the Lee optimized profile. This is the first large area warpage measurement system that can simulate a convective reflow process. This is important because convective heating does not induce large temperature gradients through the thickness of PWBs, PWBAs and chip packages which will inflate warpage measurement results. As a result of this dissertation, the AEPL shadow/projection warpage measurement system can produce more accurate warpage measurement results.

2. A CFD model was developed to determine oven parameter settings to enable the implemented convective heating system to simulate reflow profiles with high ramp rates. An example of suitable parameter settings to produce a PWB ramp rate of 2 ^{o}C/second are a heater power of 68 kW, a heater surface area of 2.32 m^2 and a system volume of 0.33 m^3. The CFD model is important because the results can be implemented to enable the shadow/projection moiré warpage measurement system to simulate high ramp rate temperature profiles such as the RDRP profile. If the shadow/projection moiré system can simulate RDRP reflow profiles in addition to the Lee optimized reflow profile, the system may be used to monitor PWB/PWBA/chip package warpage during any type of reflow process.

3. An automated chip package segmentation algorithm was developed for use with the projection moiré measurement technique. The developed algorithm can segment up to two chip packages from a PWB such that the PWB warpage and chip package warpage can be determined separately. Without the development of the chip package detection algorithm in this thesis, the only

way to determine PWB and chip package warpage would be to manually segment the chip package locations using the gerber file. A manual segementation would have to be performed after every measurement and may not be accurate. The developed algorithm is fully automated and the experimenter does not need to know the exact chip package locations or the chip package sizes during the experimental process. The developed and implemented chip package detection algorithm enables the projection moiré system to measure the warpage of populated PWBs, which is of importance to the electronic packaging industry. Other than the reseach performed in the AEPL, no work has been done to experimentalkly study the warpage of populated PWBs. This is mainly due to the limitations of currently available warpage measurement systems. The research presented in this dissertation has filled the gap.

4. A repeatability study was performed on the projection moiré system. A goal of the AEPL is to develop warpage measurement systems that can be used in an online manufacturing environment. In order for the projection moiré system to satisfy this requirement, it must be repeatable.

5. The projection moiré measurement technique was used to measure the warpage of PWBs populated with PBGA packages during a convective heating process. This is the first work that experimentally studies the behavior of populated PWBAs. The experimental study was made possible by the researched performed in this thesis.

6. A finite element model was developed to study the effect of PBGA package locations on PWB warpage. Outside of the work done in the AEPL, there has been no work done in this area. The results presented may be useful for PWBA layout designers interested in minimizing warpage during the PWBA manufacturing process, although more studies are needed to see if the results presented in this dissertation hold true for any type of PWBA.

8.3 Recommendations for Future Work

After the completion of this research, there are still many facets of PWB/PWBA /chip package warpage measurement system development and PWB/PWBA/chip package warpage measurement study that are left unexplored. Some recommendations for future work are listed below.

1. The oven parameter settings to enable the convective heating system to simulate high ramp rate reflow profiles should be implemented. This would require purchasing new heaters, and reducing the volume of the entire oven system.
2. The cooling process of the implemented convective system should be automated. This would require the addition of actuators to the air dampers in the ductwork. An automated cooling process would enable the entire heating and cooling process to be peformed at the computer. Automation of the cooling process and recommendation 1 could perhaps form the basis of a masters thesis.

3. A fully automated projection moiré system is needed so that the system has a unified computer system. Currently, whenever a projection moiré measurement is performed during infrared or convective heating, two computers must be operated simultaneously. For experimental ease and efficiency, merging the projection moiré measurement process with the infrared/convective heating process would streamline the projection moiré measurement process.

4. The chip package detection algorithm implemented in this thesis could be developed further to handle many chip packages using optimized programming. Also, the algorithm could be developed to handle chip packages assembled at an angle to the PWB edges.

5. More PBGA package layout configurations could be studied. Perhaps, the finite element model and experimental test vehicles could be used to study the effects on PWB warpage of chip packages assembled on both sides of the PWB. Also, other types of PWBs and electronic components should be tested as the relative stiffnesses between the two may affect the observations made in this dissertation.

6. A comprehensive study is needed to interpret the meaning of quantitative PWBA warpage results and their implications on the reliability of the assembly. For example, a correlation between PWB warpage and solder joint reliability would provide a useful guideline for emerging PWBA designs, provided that the PWB warpage can be easily determined using experimental, analytical or numerical approaches.

APPENDIX A

FLUENT CODE AND MATERIAL PROPERTIES

In this appendix, the material properties used in the CFD model as well as the geometry and meshing GAMBIT/FLUENT code are given.

A.1 CFD Model Material Properties

The temperature dependent thermal properties for air are shown in Table A.1 [71].

Table A.1. Temperature dependent thermal properties for air

Temperature (K)	Density (kg/m^3)	Specific Heat (J/kg K)	Thermal Conductivity (W/m K)	Viscosity (Ns/m^2)
300	1.1614	1007	0.0263	1.846E-05
350	0.9950	1009	0.0300	2.082E-05
400	0.8711	1014	0.0338	2.301E-05
450	0.7740	1021	0.0373	2.507E-05
500	0.6964	1030	0.0407	2.701E-05
550	0.6329	1040	0.0439	2.884E-05
600	0.5804	1051	0.0469	3.058E-05
650	0.5356	1063	0.0497	3.225E-05
700	0.4975	1075	0.0524	3.388E-05
750	0.4643	1087	0.0549	3.546E-05
800	0.4354	1099	0.0573	3.698E-05
850	0.4097	1110	0.0596	3.843E-05
900	0.3868	1121	0.0620	3.981E-05
950	0.3666	1131	0.0643	4.113E-05
1000	0.3482	1141	0.0667	4.244E-05

The temperature dependent thermal properties for AISI 1010 carbon steel are shown in Table A.2 [71].

Table A.2 Temperature dependent thermal properties for AISI 1010 carbon steel

Temperature (K)	Density (kg/m^3)	Specific Heat (J/kg K)	Thermal Conductivity (W/m K)
300	7854	434	60.5
400		487	56.7
600		559	48.0
800		685	39.2
1000		1169	30.0

The temperature dependent thermal properties for AISI 304 stainless steel are shown in Table A.3 [71].

Table A.3. Temperature dependent thermal properties for AISI 304 stainless steel

Temperature (K)	Density (kg/m^3)	Specific Heat (J/kg K)	Thermal Conductivity (W/m K)
300	7900	477	14.9
400		515	16.6
600		557	19.8
800		582	22.6
1000		611	25.4

A.2 CFD Model Geometry and Meshing Code in GAMBIT/FLUENT

The code used for modeling and meshing the oven geometry as well as code to extract temperatures versus time of the PWB is included below. Note that boundary condition application, loading and solving were all done using FLUENT's graphical user interface (GUI).

```
/Author: Reinhard Powell
/This file contains the geometry and meshing for geometry of laboratory oven.
/The oven volume and heater surface area are changed with simple modifications of this
file.

/ oven chamber vertices and edges
vertex create "oven_bot_leftz+" coordinates -19 -7 15
vertex create "oven_bot_leftz-" coordinates -19 -7 0
vertex create "oven_bot_rghtz+" coordinates 15 -7 15
vertex create "oven_bot_rghtz-" coordinates 15 -7 0
vertex create "oven_top_leftz+" coordinates -19 7 15
vertex create "oven_top_leftz-" coordinates -19 7 0
vertex create "oven_top_rghtz+" coordinates 15 7 15
vertex create "oven_top_rghtz-" coordinates 15 7 0
vertex create "oven_midt_rghtz-" coordinates 15 1.75 0
vertex create "oven_midb_rghtz-" coordinates 15 -4.25 0
vertex create "ovenwall_topz-" coordinates -15 7 0
vertex create "ovenwall_topz+" coordinates -15 7 15
vertex create "ovenwall_botz+" coordinates -15 -7 15
vertex create "ovenwall_back_top" coordinates -15 4 0
vertex create "ovenwall_back_bot" coordinates -15 -4 0
vertex create "ovenwall_back_cnt" coordinates -15 0 0

edge create "edge1" arc radius 4 startangle 0 endangle 180 center "ovenwall_back_cnt"
yzplane
edge create "edge2" straight "oven_bot_leftz+" "ovenwall_botz+"
edge create "edge3" straight "oven_top_leftz+" "ovenwall_topz+"
edge create "edge4" straight "oven_top_leftz-" "ovenwall_topz-"
edge create "edge5" straight "oven_top_leftz+" "oven_top_leftz-"
edge create "edge6" straight "oven_top_rghtz+" "oven_top_rghtz-"
edge create "edge7" straight "oven_bot_rghtz+" "oven_bot_rghtz-"
edge create "edge8" straight "oven_bot_leftz+" "oven_top_leftz+"
edge create "edge9" straight "oven_bot_rghtz+" "oven_top_rghtz+"
edge create "edge10" straight "oven_bot_leftz-" "oven_top_leftz-"
edge create "edge11" straight "oven_bot_rghtz-" "oven_midb_rghtz-"
edge create "edge12" straight "oven_midb_rghtz-" "oven_midt_rghtz-"
edge create "edge13" straight "oven_midt_rghtz-" "oven_top_rghtz-"
edge create "edge14" straight "ovenwall_botz+" "ovenwall_topz+"
edge create "edge15" straight "ovenwall_topz+" "ovenwall_topz-"
edge create "edge16" straight "ovenwall_botz+" "oven_bot_rghtz+"
edge create "edge17" straight "ovenwall_topz+" "oven_top_rghtz+"
edge create "edge18" straight "ovenwall_topz-" "oven_top_rghtz-"

/ duct 1 vertices and faces
vertex create "duct1_top_rghtz-" coordinates -15 -7 0
vertex create "duct1_top_rghtz+" coordinates -15 -7 7.25
vertex create "duct1_top_leftz+" coordinates -19 -7 7.25
vertex create "duct1_bot_leftz+" coordinates -19 -20.5 7.25
vertex create "duct1_bot_leftz-" coordinates -19 -20.5 0
vertex create "duct1_bot_rghtz+" coordinates -15 -20.5 7.25
vertex create "duct1_bot_rghtz-" coordinates -15 -20.5 0

edge create "edge20" straight "oven_bot_leftz-" "duct1_top_rghtz-"
edge create "edge21" straight "duct1_top_leftz+" "duct1_top_rghtz+"
edge create "edge22" straight "duct1_bot_leftz+" "duct1_bot_rghtz+"
edge create "edge23" straight "duct1_bot_leftz-" "duct1_bot_rghtz-"
edge create "edge24" straight "duct1_top_leftz+" "oven_bot_leftz-"
edge create "edge25" straight "duct1_top_rghtz+" "duct1_top_rghtz-"
edge create "edge26" straight "duct1_bot_rghtz+" "duct1_bot_rghtz-"
edge create "edge27" straight "duct1_bot_leftz+" "duct1_bot_leftz-"
edge create "edge28" straight "duct1_bot_leftz+" "duct1_top_leftz+"
edge create "edge29" straight "duct1_bot_leftz-" "oven_bot_leftz-"
edge create "edge30" straight "duct1_top_rghtz-" "oven_bot_rghtz-"
edge create "edge32" straight "oven_bot_leftz-" "duct1_top_leftz+"
edge create "edge33" straight "duct1_top_leftz+" "oven_bot_leftz+"
edge create "edge34" straight "duct1_top_rghtz+" "ovenwall_botz+"
edge create "edge35" straight "ovenwall_topz-" "ovenwall_back_top"
edge create "edge36" straight "ovenwall_back_bot" "duct1_top_rghtz-"

/wall face
```

```
face create "wallface" wireframe "edge35" "edge15" "edge14" "edge34" "edge25" "edge36"
"edge1" real

/duct 2 vertices and edges
vertex create "duct2_top_leftz+" coordinates -15 -15.5 7.25
vertex create "duct2_top_leftz-" coordinates -15 -15.5 0
vertex create "duct2_top_rghtz+" coordinates 13 -15.5 3.75
vertex create "duct2_top_rghtz-" coordinates 13 -15.5 0
vertex create "duct2_bot_rghtz+" coordinates 13 -20.5 3.75
vertex create "duct2_bot_rghtz-" coordinates 13 -20.5 0

edge create "edge40" straight "duct1_top_rghtz-" "duct2_top_leftz-"
edge create "edge41" straight "duct1_top_rghtz+" "duct2_top_leftz+"
edge create "edge42" Straight "duct2_top_leftz-" "duct1_bot_rghtz-"
edge create "edge43" Straight "duct2_top_leftz+" "duct1_bot_rghtz+"
edge create "edge44" straight "duct2_top_leftz+" "duct2_top_leftz-"
edge create "edge45" straight "duct2_top_rghtz+" "duct2_top_rghtz-"
edge create "edge46" straight "duct2_bot_rghtz+" "duct2_bot_rghtz-"
edge create "edge47" straight "duct2_top_leftz+" "duct2_top_rghtz+"
edge create "edge48" straight "duct2_top_leftz-" "duct2_top_rghtz-"
edge create "edge49" straight "duct1_bot_rghtz+" "duct2_bot_rghtz+"
edge create "edge50" straight "duct1_bot_rghtz-" "duct2_bot_rghtz-"
edge create "edge51" straight "duct2_bot_rghtz+" "duct2_top_rghtz+"
edge create "edge52" straight "duct2_top_rghtz-" "duct2_bot_rghtz-"

/duct 1 faces and volume
face create "duct1lface" wireframe "edge28" "edge24" "edge29" "edge27" real
face create "duct1rtface" wireframe "edge25" "edge40" "edge41" "edge44" real
face create "duct1fface" wireframe "edge28" "edge41" "edge21" "edge22" "edge43" real
face create "duct1baface" wireframe "edge20" "edge29" "edge40" "edge42" "edge23" real
face create "duct1boface" wireframe "edge26" "edge23" "edge27" "edge22" real
face create "duct1tface" wireframe "edge25" "edge20" "edge24" "edge21" real
face create "duct1rbface" wireframe "edge44" "edge42" "edge43" "edge26" real
volume create "duct1" stitch "duct1tface" "duct1lface" "duct1rtface" "duct1rbface"
"duct1fface" "duct1baface" "duct1boface"

/duct 2 faces and volume
face create "duct2rface" wireframe "edge45" "edge52" "edge51" "edge46" real
face create "duct2fface" wireframe "edge43" "edge47" "edge51" "edge49" real
face create "duct2baface" wireframe "edge42" "edge48" "edge50" "edge52" real
face create "duct2boface" wireframe "edge49" "edge50" "edge46" "edge26" real
face create "duct2tface" wireframe "edge45" "edge48" "edge44" "edge47" real
volume create "duct2" stitch "duct1rbface" "duct2rface" "duct2fface" "duct2baface"
"duct2boface" "duct2tface"

/transition 1
vertex create "tra_cntz-" coordinates 21 -18 0
vertex create "tra_top" coordinates 21 -14 0
vertex create "tra_bot" coordinates 21 -22 0
vertex create "tra_up" coordinates 21 -15.1715728753 2.82842712474
vertex create "tra_dwn" coordinates 21 -20.8284271247 2.82842712474

edge create "edge60" arc radius 4 startangle 0 endangle 45 center "tra_cntz-" yzplane
edge create "edge61" arc radius 4 startangle 45 endangle 135 center "tra_cntz-" yzplane
edge create "edge62" arc radius 4 startangle 135 endangle 180 center "tra_cntz-" yzplane
edge create "edge63" straight "duct2_top_rghtz-" "tra_top"
edge create "edge64" straight "duct2_top_rghtz+" "tra_up"
edge create "edge65" straight "duct2_bot_rghtz+" "tra_dwn"
edge create "edge66" straight "duct2_bot_rghtz-" "tra_bot"
edge create "edge67" straight "tra_top" "tra_bot"

face create "trans1rface" wireframe "edge60" "edge61" "edge62" "edge67" real
face create "trans1tface" wireframe "edge63" "edge45" "edge64" "edge60" real
face create "trans1fface" wireframe "edge64" "edge51" "edge65" "edge61" real
face create "trans1boface" wireframe "edge46" "edge66" "edge65" "edge62" real
face create "trans1baface" wireframe "edge52" "edge63" "edge67" "edge66" real
volume create "transition1" stitch "trans1rface" "trans1tface" "trans1fface"
"trans1boface" "trans1baface" "duct2rface"

/elbow 1
vertex create "el1cnt" coordinates 21 -30 0
```

```
vertex create "el1end" coordinates 33 -30 0
edge create "edge70" arc radius 12 startangle 0 endangle 90 center "el1cnt" xyplane

/heater duct
vertex create "hduct_top_leftz+" coordinates 15 1.75 10
vertex create "hduct_top_rghtz-" coordinates 28 1.75 0
vertex create "hduct_top_rghtz+" coordinates 28 1.75 10
vertex create "hduct_bot_leftz+" coordinates 15 -4.25 10
vertex create "hduct_bot_rghtz-" coordinates 28 -4.25 0
vertex create "hduct_bot_rghtz+" coordinates 28 -4.25 10

edge create "edge75" straight "oven_midt_rghtz-" "hduct_top_rghtz-"
edge create "edge76" straight "hduct_top_leftz+" "hduct_top_rghtz+"
edge create "edge77" straight "oven_midb_rghtz-" "hduct_bot_rghtz-"
edge create "edge78" straight "hduct_bot_leftz+" "hduct_bot_rghtz+"
edge create "edge79" straight "oven_midt_rghtz-" "hduct_top_leftz+"
edge create "edge80" straight "oven_midb_rghtz-" "hduct_bot_leftz+"
edge create "edge81" straight "hduct_top_leftz+" "hduct_bot_leftz+"
edge create "edge82" straight "hduct_top_rghtz+" "hduct_bot_rghtz+"

/fan plenum and vanes
vertex create "plen_top_left2" coordinates 28 1.75 3
vertex create "plen_top_left3" coordinates 28 1.75 6
vertex create "plen_bot_left2" coordinates 28 -4.25 3
vertex create "plen_bot_left3" coordinates 28 -4.25 6
vertex create "plen_top_rghtz-" coordinates 41 1.75 0
vertex create "plen_top_rght2" coordinates 41 1.75 0.9375
vertex create "plen_top_rght3" coordinates 41 1.75 1.875
vertex create "plen_top_rghtz+" coordinates 41 1.75 2.8125
vertex create "plen_bot_rghtz-" coordinates 41 -4.25 0
vertex create "plen_bot_rght2" coordinates 41 -4.25 0.9375
vertex create "plen_bot_rght3" coordinates 41 -4.25 1.875
vertex create "plen_bot_rghtz+" coordinates 41 -4.25 2.8125

edge create "edge84" straight "plen_bot_rghtz-" "plen_bot_rght2"
edge create "edge85" straight "plen_bot_rght2" "plen_bot_rght3"
edge create "edge86" straight "plen_bot_rght3" "plen_bot_rghtz+"
edge create "edge87" straight "plen_top_rghtz-" "plen_top_rght2"
edge create "edge88" straight "plen_top_rght2" "plen_top_rght3"
edge create "edge89" Straight "plen_top_rght3" "plen_top_rghtz+"
edge create "edge90" straight "plen_bot_left2" "plen_bot_left3"
edge create "edge91" straight "hduct_top_rghtz-" "hduct_bot_rghtz-"
edge create "edge92" straight "plen_top_rghtz+" "plen_bot_rghtz+"
edge create "edge93" straight "plen_top_rghtz-" "plen_bot_rghtz-"
edge create "edge94" straight "hduct_top_rghtz-" "plen_top_rghtz-"
edge create "edge95" straight "hduct_top_rghtz+" "plen_top_rghtz+"
edge create "edge96" straight "hduct_bot_rghtz-" "plen_bot_rghtz-"
edge create "edge97" straight "hduct_bot_rghtz+" "plen_bot_rghtz+"
edge create "edge98" straight "hduct_top_rghtz-" "plen_top_left2"
edge create "edge99" straight "plen_top_left2" "plen_top_left3"
edge create "edge100" straight "plen_top_left3" "hduct_top_rghtz+"
edge create "edge101" straight "hduct_bot_rghtz-" "plen_bot_left2"
edge create "edge102" straight "plen_top_left2" "plen_top_rght2"
edge create "edge103" straight "plen_top_left3" "plen_top_rght3"
edge create "edge104" straight "plen_bot_left2" "plen_bot_rght2"
edge create "edge105" straight "plen_bot_left3" "plen_bot_rght3"
edge create "edge106" straight "plen_top_left2" "plen_bot_left2"
edge create "edge107" straight "plen_top_left3" "plen_bot_left3"
edge create "edge108" straight "plen_top_rght2" "plen_bot_rght2"
edge create "edge109" straight "plen_top_rght3" "plen_bot_rght3"
edge create "edge110" straight "plen_bot_left3" "hduct_bot_rghtz+"

/middle vane
face create "midvane" wireframe "edge102" "edge106" "edge104" "edge108" real

/outer vane
face create "outervane" wireframe "edge103" "edge107" "edge105" "edge109" real

/plenum faces and volume
face create "plenlface1" wireframe "edge98" "edge91" "edge106" "edge101" real
face create "plenlface2" wireframe "edge99" "edge107" "edge106" "edge90" real
```

```
face create "plenlface3" wireframe "edge82" "edge100" "edge107" "edge110" real
face create "plenriface1" wireframe "edge93" "edge87" "edge108" "edge84" real
face create "plenriface2" wireframe "edge88" "edge109" "edge108" "edge85" real
face create "plenriface3" wireframe "edge92" "edge89" "edge109" "edge86" real
face create "plentface1" wireframe "edge94" "edge98" "edge102" "edge87" real
face create "plentface2" wireframe "edge99" "edge103" "edge102" "edge88" real
face create "plentface3" wireframe "edge100" "edge103" "edge95" "edge89" real
face create "plenfface" wireframe "edge95" "edge82" "edge97" "edge92" real
face create "plenbaface1" wireframe "edge94" "edge91" "edge96" "edge93" real
face create "plenboface1" wireframe "edge96" "edge101" "edge104" "edge84" real
face create "plenboface2" wireframe "edge90" "edge104" "edge105" "edge85" real
face create "plenboface3" wireframe "edge110" "edge105" "edge97" "edge86" real
volume create "plenum1" stitch "plenlface1" "plenriface1" "plentface1" "plenboface1"
"midvane" "plenbaface1"
volume create "plenum2" stitch "plenlface2" "plenriface2" "plentface2" "plenboface2"
"midvane" "outervane"
volume create "plenum3" stitch "plenlface3" "plenriface3" "plentface3" "plenboface3"
"plenfface" "outervane"

/addin
vertex create "addin_top_rghtz-" coordinates 42 1.75 0
vertex create "addin_top_rghtz+" coordinates 42 1.75 2.8125
vertex create "addin_bot_rghtz-" coordinates 42 -4.25 0
vertex create "addin_bot_rghtz+" coordinates 42 -4.25 2.8125

edge create "edge1a" straight "plen_top_rghtz+" "addin_top_rghtz+"
edge create "edge1b" straight "plen_top_rghtz-" "addin_top_rghtz-"
edge create "edge1c" straight "plen_bot_rghtz+" "addin_bot_rghtz+"
edge create "edge1d" straight "plen_bot_rghtz-" "addin_bot_rghtz-"
edge create "edge1e" straight "addin_bot_rghtz+" "addin_top_rghtz+"
edge create "edge1f" straight "addin_bot_rghtz-" "addin_top_rghtz-"
edge create "edge1g" straight "addin_bot_rghtz+" "addin_bot_rghtz-"
edge create "edge1h" straight "addin_top_rghtz+" "addin_top_rghtz-"

face create "addfface" wireframe "edge1a" "edge1e" "edge1c" "edge92" real
face create "addbaface" wireframe "edge1b" "edge1d" "edge93" "edge1f" real
face create "addtface" wireframe "edge1a" "edge1h" "edge1b" "edge87" "edge88" "edge89"
real
face create "addboface" wireframe "edge86" "edge85" "edge84" "edge1d" "edge1c" "edge1g"
real
face create "blower" wireframe "edge1e" "edge1h" "edge1f" "edge1g" real
volume create "addin" stitch "addfface" "addbaface" "addtface" "addboface" "blower"
"plenriface1" "plenriface2" "plenriface3"

/heater duct faces and volume
face create "hductfface" wireframe "edge76" "edge81" "edge78" "edge82" real
face create "hductbaface" wireframe "edge75" "edge12" "edge77" "edge91" real
face create "hductlface" wireframe "edge79" "edge12" "edge81" "edge80" real
face create "hducttface" wireframe "edge75" "edge79" "edge76" "edge100" "edge99" "edge98"
real
face create "hductboface" wireframe "edge78" "edge80" "edge110" "edge90" "edge101"
"edge77" real

/circuit board sample
vertex create "board_bot_leftz-" coordinates -2.75 4.5 0
vertex create "board_bot_leftz+" coordinates -2.75 4.5 4
vertex create "board_bot_rghtz-" coordinates 2.75 4.5 0
vertex create "board_bot_rghtz+" coordinates 2.75 4.5 4
vertex create "board_top_leftz-" coordinates -2.75 4.52484251968 0
vertex create "board_top_leftz+" coordinates -2.75 4.52484251968 4
vertex create "board_top_rghtz-" coordinates 2.75 4.52484251968 0
vertex create "board_top_rghtz+" coordinates 2.75 4.52484251968 4

edge create "edge117" straight "board_bot_leftz-" "board_bot_rghtz-"
edge create "edge118" straight "board_bot_leftz+" "board_bot_rghtz+"
edge create "edge120" straight "board_bot_leftz-" "board_bot_leftz+"
edge create "edge122" straight "board_bot_rghtz-" "board_bot_rghtz+"
edge create "edge116" straight "board_top_leftz-" "board_top_rghtz-"
edge create "edge119" straight "board_top_leftz+" "board_top_rghtz+"
edge create "edge121" straight "board_top_leftz-" "board_top_leftz+"
edge create "edge123" straight "board_top_rghtz-" "board_top_rghtz+"
```

```
edge create "edge124" straight "board_top_rghtz-" "board_bot_rghtz-"
edge create "edge125" straight "board_top_rghtz+" "board_bot_rghtz+"
edge create "edge126" straight "board_top_leftz-" "board_bot_leftz-"
edge create "edge127" straight "board_top_leftz+" "board_bot_leftz+"

/oven chamber faces
face create "ovenrface" wireframe "edge6" "edge13" "edge79" "edge9" "edge7" "edge11"
"edge80" "edge81" real
face create "oventface1" wireframe "edge18" "edge17" "edge6" "edge15" real
face create "oventface2" wireframe "edge4" "edge15" "edge5" "edge3" real
face create "ovenboface1" wireframe "edge34" "edge30" "edge7" "edge25" "edge16" real
face create "ovenboface2" wireframe "edge34" "edge2" "edge33" "edge21" real
face create "ovenfface1" wireframe  "edge9" "edge17" "edge14" "edge16" real
face create "ovenfface2" wireframe  "edge8" "edge3" "edge14" "edge2" real
face create "ovenbaface" wireframe "edge18" "edge4" "edge10" "edge20" "edge30" "edge12"
"edge11" "edge13" real
face create "ovenlface" wireframe "edge5" "edge10" "edge24" "edge33" "edge8" real

/board face and volume
face create "boardboface" wireframe "edge122" "edge117" "edge118" "edge120" real
face create "boardtface" wireframe "edge119" "edge121" "edge116" "edge123" real
face create "boardrface" wireframe "edge125" "edge123" "edge124" "edge122" real
face create "boardlface" wireframe "edge121" "edge120" "edge126" "edge127" real
face create "boardfface" wireframe "edge119" "edge118" "edge125" "edge127" real
face create "boardbaface" wireframe "edge116" "edge126" "edge117" "edge124" real
volume create "board" stitch "boardboface" "boardtface" "boardrface" "boardlface"
"boardfface" "boardbaface"

/oven volume
volume create "ovenchamber" stitch "hductlface" "ovenlface" "ovenrface" "oventface1" \
"oventface2"  "ovenboface1"  "ovenboface2"  "duct1tface"  "ovenbaface"  "ovenfface1"
"ovenfface2"
volume split "ovenchamber" faces "wallface" connected
volume subtract "ovenchamber" volumes "board"

/transition 2
vertex create "tra2_cntz-" coordinates 49 -1.25 0
vertex create "tra2_top" coordinates 49 2.75 0
vertex create "tra2_bot" coordinates 49 -5.25 0
vertex create "tra2_up" coordinates 49 1.57842712474 2.82842712474
vertex create "tra2_dwn" coordinates 49 -4.07842712474 2.82842712474

edge create "edge135" arc radius 4 startangle 0 endangle 45 center "tra2_cntz-" yzplane
edge create "edge136" arc radius 4 startangle 45 endangle 135 center "tra2_cntz-" yzplane
edge create "edge137" arc radius 4 startangle 135 endangle 180 center "tra2_cntz-"
yzplane
edge create "edge138" straight "addin_top_rghtz-" "tra2_top"
edge create "edge139" straight "addin_top_rghtz+" "tra2_up"
edge create "edge140" straight "addin_bot_rghtz+" "tra2_dwn"
edge create "edge141" straight "addin_bot_rghtz-" "tra2_bot"
edge create "edge143" straight "tra2_top" "tra2_bot"

face create "trans2rface" wireframe "edge143" "edge135" "edge136" "edge137" real
face create "trans2tface" wireframe "edge1h" "edge139" "edge138" "edge135" real
face create "trans2fface" wireframe "edge1e" "edge139" "edge136" "edge140" real
face create "trans2boface" wireframe "edge137" "edge141" "edge140" "edge1g" real
face create "trans2baface" wireframe "edge138" "edge1f" "edge143" "edge141" real
volume  create  "transition2"  stitch  "trans2rface"  "trans2tface"  "trans2fface"
"trans2boface" "trans2baface" "blower"

/elbow 2
vertex create "el2cnt" coordinates 49 -13.25 0
vertex create "el2end" coordinates 61 -13.25 0
edge create "edge172" arc radius 12 startangle 0 endangle 90 center "el2cnt" xyplane

/rest of ductwork
vertex create "vert1" coordinates 33 -32.625 0
vertex create "vert2" coordinates 37 -36.625 0
vertex create "vert3" coordinates 37 -32.625 0
vertex create "vert4" coordinates 57 -36.625 0
vertex create "vert5" coordinates 61 -32.625 0
```

```
vertex create "vert6" coordinates 57 -32.625 0

edge create "edge150" straight "vert5" "el2end"
edge create "edge151" straight "vert1" "el1end"
edge create "edge152" straight "vert2" "vert4"
edge create "edge153" arc radius 4 startangle 180 endangle 270 center "vert3" xyplane
edge create "edge154" arc radius 4 startangle 270 endangle 360 center "vert6" xyplane

volume create "volume1" rotate "trans1rface" onedge "edge70" reverse draft 0 extended

face modify "face.66" label "face1"
volume create "volume2" translate "face1" onedge "edge151" reverse
face modify "face.72" label "face2"
volume create "volume3" rotate "face2" onedge "edge153" draft 0 extended
face modify "face.75" label "face3"
volume create "volume4" translate "face3" onedge "edge152"
face modify "face.82" label "face4"
volume create "volume5" rotate "face4" onedge "edge154" draft 0 extended
volume create "volume7" rotate "trans2rface" onedge "edge172" reverse draft 0 extended

/create volume 6
edge create "edge160" straight "vert6" "vertex.129"
edge create "edge161" straight "vertex.131" "vertex.127"
edge create "edge162" straight "vertex.132" "vertex.128"
edge create "edge163" straight "vertex.130" "vertex.126"

face create "vol6curm" wireframe "edge.181" "edge161" "edge162" "edge.173" real
face create "vol6curl" wireframe "edge160" "edge.177" "edge161" "edge.169" real
face create "vol6curr" wireframe "edge.178" "edge162" "edge163" "edge.170" real
face create "vol6ba" wireframe "edge.174" "edge160" "edge.168" "edge163" real
face modify "face.91" label "vol6tface"
face modify "face.85" label "vol6bface"

volume create "volume6" stitch "vol6tface" "vol6bface" "vol6curm" "vol6curl" "vol6curr"
"vol6ba"

/modify elbow 1 faces
face modify "face.64" label "elb1baface"
face modify "face.65" label "elb1curbface"
face modify "face.67" label "elb1curtface"
face modify "face.68" label "elb1curmface"

/modify small straight duct faces
face modify "face.69" label "smstrabaface"
face modify "face.70" label "smstracurlface"
face modify "face.71" label "smstracurrface"
face modify "face.73" label "smstracurmface"

/modify sharp 90 elbow 1 faces
face modify "face.74" label "shel1baface"
face modify "face.76" label "shel1curtface"
face modify "face.77" label "shel1curbface"
face modify "face.78" label "shel1curmface"

/modify straight horizontal round duct
face modify "face.79" label "hordubaface"
face modify "face.81" label "horducurtface"
face modify "face.80" label "horducurbface"
face modify "face.83" label "horducurmface"

/modify sharp 90 elbow 2 faces
face modify "face.84" label "shel2baface"
face modify "face.86" label "shel2curtface"
face modify "face.87" label "shel2curbface"
face modify "face.88" label "shel2curmface"

/modify elbow 2 faces
face modify "face.89" label "elb2baface"
face modify "face.92" label "elb2curtface"
face modify "face.90" label "elb2curbface"
face modify "face.93" label "elb2curmface"
```

```
/heaters
/heater 1
vertex create "ver1a1" coordinates 15.6875 0.3125 0
vertex create "ver1a2" coordinates 15.6875 0.3125 8.125
vertex create "ver1a3" coordinates 15.875 0.3125 0
vertex create "ver1a4" coordinates 15.5 0.3125 0
vertex create "ver1a5" coordinates 15.875 0.3125 8.125
vertex create "ver1a6" coordinates 15.5 0.3125 8.125
edge create "edge1a1" arc radius 0.1875 startangle 0 endangle 180 center "ver1a1" xyplane
edge create "edge1a2" arc radius 0.1875 startangle 180 endangle 360 center "ver1a1"
xyplane
edge create "edge1a3" arc radius 0.1875 startangle 0 endangle 180 center "ver1a2" xyplane
edge create "edge1a4" arc radius 0.1875 startangle 180 endangle 360 center "ver1a2"
xyplane
edge create "edge1a5" straight "ver1a3" "ver1a5"
edge create "edge1a6" straight "ver1a4" "ver1a6"
face create "h1abaface" wireframe "edge1a1" "edge1a2" real
face create "h1afface" wireframe "edge1a3" "edge1a4" real
face create "h1atface" wireframe "edge1a1" "edge1a3" "edge1a5" "edge1a6" real
face create "h1abface" wireframe "edge1a2" "edge1a4" "edge1a5" "edge1a6" real
volume create "heater1a" stitch "h1abaface" "h1afface" "h1atface" "h1abface"

vertex create "ver1b1" coordinates 15.6875 -1.0625 0
vertex create "ver1b2" coordinates 15.6875 -1.0625 8.125
vertex create "ver1b3" coordinates 15.875 -1.0625 0
vertex create "ver1b4" coordinates 15.5 -1.0625 0
vertex create "ver1b5" coordinates 15.875 -1.0625 8.125
vertex create "ver1b6" coordinates 15.5 -1.0625 8.125
edge create "edge1b1" arc radius 0.1875 startangle 0 endangle 180 center "ver1b1" xyplane
edge create "edge1b2" arc radius 0.1875 startangle 180 endangle 360 center "ver1b1"
xyplane
edge create "edge1b3" arc radius 0.1875 startangle 0 endangle 180 center "ver1b2" xyplane
edge create "edge1b4" arc radius 0.1875 startangle 180 endangle 360 center "ver1b2"
xyplane
edge create "edge1b5" straight "ver1b3" "ver1b5"
edge create "edge1b6" straight "ver1b4" "ver1b6"
face create "h1bbaface" wireframe "edge1b1" "edge1b2" real
face create "h1bfface" wireframe "edge1b3" "edge1b4" real
face create "h1btface" wireframe "edge1b1" "edge1b3" "edge1b5" "edge1b6" real
face create "h1bbface" wireframe "edge1b2" "edge1b4" "edge1b5" "edge1b6" real
volume create "heater1b" stitch "h1bbaface" "h1bfface" "h1btface" "h1bbface"

vertex create "ver1c1" coordinates 15.6875 -2.4375 0
vertex create "ver1c2" coordinates 15.6875 -2.4375 8.125
vertex create "ver1c3" coordinates 15.875 -2.4375 0
vertex create "ver1c4" coordinates 15.5 -2.4375 0
vertex create "ver1c5" coordinates 15.875 -2.4375 8.125
vertex create "ver1c6" coordinates 15.5 -2.4375 8.125
edge create "edge1c1" arc radius 0.1875 startangle 0 endangle 180 center "ver1c1" xyplane
edge create "edge1c2" arc radius 0.1875 startangle 180 endangle 360 center "ver1c1"
xyplane
edge create "edge1c3" arc radius 0.1875 startangle 0 endangle 180 center "ver1c2" xyplane
edge create "edge1c4" arc radius 0.1875 startangle 180 endangle 360 center "ver1c2"
xyplane
edge create "edge1c5" straight "ver1c3" "ver1c5"
edge create "edge1c6" straight "ver1c4" "ver1c6"
face create "h1cbaface" wireframe "edge1c1" "edge1c2" real
face create "h1cfface" wireframe "edge1c3" "edge1c4" real
face create "h1ctface" wireframe "edge1c1" "edge1c3" "edge1c5" "edge1c6" real
face create "h1cbface" wireframe "edge1c2" "edge1c4" "edge1c5" "edge1c6" real
volume create "heater1c" stitch "h1cbaface" "h1cfface" "h1ctface" "h1cbface"

vertex create "ver1d1" coordinates 15.6875 -3.8125 0
vertex create "ver1d2" coordinates 15.6875 -3.8125 8.125
vertex create "ver1d3" coordinates 15.875 -3.8125 0
vertex create "ver1d4" coordinates 15.5 -3.8125 0
vertex create "ver1d5" coordinates 15.875 -3.8125 8.125
vertex create "ver1d6" coordinates 15.5 -3.8125 8.125
edge create "edge1d1" arc radius 0.1875 startangle 0 endangle 180 center "ver1d1" xyplane
```

```
edge create "edge1d2" arc radius 0.1875 startangle 180 endangle 360 center "ver1d1"
xyplane
edge create "edge1d3" arc radius 0.1875 startangle 0 endangle 180 center "ver1d2" xyplane
edge create "edge1d4" arc radius 0.1875 startangle 180 endangle 360 center "ver1d2"
xyplane
edge create "edge1d5" straight "ver1d3" "ver1d5"
edge create "edge1d6" straight "ver1d4" "ver1d6"
face create "h1dbaface" wireframe "edge1d1" "edge1d2" real
face create "h1dfface" wireframe "edge1d3" "edge1d4" real
face create "h1dtface" wireframe "edge1d1" "edge1d3" "edge1d5" "edge1d6" real
face create "h1dbface" wireframe "edge1d2" "edge1d4" "edge1d5" "edge1d6" real
volume create "heater1d" stitch "h1dbaface" "h1dfface" "h1dtface" "h1dbface"

/heater2
vertex create "ver2a1" coordinates 16.1875 0.8125 0
vertex create "ver2a2" coordinates 16.1875 0.8125 8.125
vertex create "ver2a3" coordinates 16.375 0.8125 0
vertex create "ver2a4" coordinates 16 0.8125 0
vertex create "ver2a5" coordinates 16.375 0.8125 8.125
vertex create "ver2a6" coordinates 16 0.8125 8.125
edge create "edge2a1" arc radius 0.1875 startangle 0 endangle 180 center "ver2a1" xyplane
edge create "edge2a2" arc radius 0.1875 startangle 180 endangle 360 center "ver2a1"
xyplane
edge create "edge2a3" arc radius 0.1875 startangle 0 endangle 180 center "ver2a2" xyplane
edge create "edge2a4" arc radius 0.1875 startangle 180 endangle 360 center "ver2a2"
xyplane
edge create "edge2a5" straight "ver2a3" "ver2a5"
edge create "edge2a6" straight "ver2a4" "ver2a6"
face create "h2abaface" wireframe "edge2a1" "edge2a2" real
face create "h2afface" wireframe "edge2a3" "edge2a4" real
face create "h2atface" wireframe "edge2a1" "edge2a3" "edge2a5" "edge2a6" real
face create "h2abface" wireframe "edge2a2" "edge2a4" "edge2a5" "edge2a6" real
volume create "heater2a" stitch "h2abaface" "h2afface" "h2atface" "h2abface"

vertex create "ver2b1" coordinates 16.1875 -0.5625 0
vertex create "ver2b2" coordinates 16.1875 -0.5625 8.125
vertex create "ver2b3" coordinates 16.375 -0.5625 0
vertex create "ver2b4" coordinates 16 -0.5625 0
vertex create "ver2b5" coordinates 16.375 -0.5625 8.125
vertex create "ver2b6" coordinates 16 -0.5625 8.125
edge create "edge2b1" arc radius 0.1875 startangle 0 endangle 180 center "ver2b1" xyplane
edge create "edge2b2" arc radius 0.1875 startangle 180 endangle 360 center "ver2b1"
xyplane
edge create "edge2b3" arc radius 0.1875 startangle 0 endangle 180 center "ver2b2" xyplane
edge create "edge2b4" arc radius 0.1875 startangle 180 endangle 360 center "ver2b2"
xyplane
edge create "edge2b5" straight "ver2b3" "ver2b5"
edge create "edge2b6" straight "ver2b4" "ver2b6"
face create "h2bbaface" wireframe "edge2b1" "edge2b2" real
face create "h2bfface" wireframe "edge2b3" "edge2b4" real
face create "h2btface" wireframe "edge2b1" "edge2b3" "edge2b5" "edge2b6" real
face create "h2bbface" wireframe "edge2b2" "edge2b4" "edge2b5" "edge2b6" real
volume create "heater2b" stitch "h2bbaface" "h2bfface" "h2btface" "h2bbface"

vertex create "ver2c1" coordinates 16.1875 -1.9375 0
vertex create "ver2c2" coordinates 16.1875 -1.9375 8.125
vertex create "ver2c3" coordinates 16.375 -1.9375 0
vertex create "ver2c4" coordinates 16 -1.9375 0
vertex create "ver2c5" coordinates 16.375 -1.9375 8.125
vertex create "ver2c6" coordinates 16 -1.9375 8.125
edge create "edge2c1" arc radius 0.1875 startangle 0 endangle 180 center "ver2c1" xyplane
edge create "edge2c2" arc radius 0.1875 startangle 180 endangle 360 center "ver2c1"
xyplane
edge create "edge2c3" arc radius 0.1875 startangle 0 endangle 180 center "ver2c2" xyplane
edge create "edge2c4" arc radius 0.1875 startangle 180 endangle 360 center "ver2c2"
xyplane
edge create "edge2c5" straight "ver2c3" "ver2c5"
edge create "edge2c6" straight "ver2c4" "ver2c6"
face create "h2cbaface" wireframe "edge2c1" "edge2c2" real
face create "h2cfface" wireframe "edge2c3" "edge2c4" real
face create "h2ctface" wireframe "edge2c1" "edge2c3" "edge2c5" "edge2c6" real
```

```
face create "h2cbface" wireframe "edge2c2" "edge2c4" "edge2c5" "edge2c6" real
volume create "heater2c" stitch "h2cbaface" "h2cfface" "h2ctface" "h2cbface"

vertex create "ver2d1" coordinates 16.1875 -3.3125 0
vertex create "ver2d2" coordinates 16.1875 -3.3125 8.125
vertex create "ver2d3" coordinates 16.375 -3.3125 0
vertex create "ver2d4" coordinates 16 -3.3125 0
vertex create "ver2d5" coordinates 16.375 -3.3125 8.125
vertex create "ver2d6" coordinates 16 -3.3125 8.125
edge create "edge2d1" arc radius 0.1875 startangle 0 endangle 180 center "ver2d1" xyplane
edge create "edge2d2" arc radius 0.1875 startangle 180 endangle 360 center "ver2d1"
xyplane
edge create "edge2d3" arc radius 0.1875 startangle 0 endangle 180 center "ver2d2" xyplane
edge create "edge2d4" arc radius 0.1875 startangle 180 endangle 360 center "ver2d2"
xyplane
edge create "edge2d5" straight "ver2d3" "ver2d5"
edge create "edge2d6" straight "ver2d4" "ver2d6"
face create "h2dbaface" wireframe "edge2d1" "edge2d2" real
face create "h2dfface" wireframe "edge2d3" "edge2d4" real
face create "h2dtface" wireframe "edge2d1" "edge2d3" "edge2d5" "edge2d6" real
face create "h2dbface" wireframe "edge2d2" "edge2d4" "edge2d5" "edge2d6" real
volume create "heater2d" stitch "h2dbaface" "h2dfface" "h2dtface" "h2dbface"

/heater3
vertex create "ver3a1" coordinates 16.6875  1.3125 0
vertex create "ver3a2" coordinates 16.6875  1.3125 8.125
vertex create "ver3a3" coordinates 16.875 1.3125 0
vertex create "ver3a4" coordinates 16.5 1.3125 0
vertex create "ver3a5" coordinates 16.875 1.3125 8.125
vertex create "ver3a6" coordinates 16.5 1.3125 8.125
edge create "edge3a1" arc radius 0.1875 startangle 0 endangle 180 center "ver3a1" xyplane
edge create "edge3a2" arc radius 0.1875 startangle 180 endangle 360 center "ver3a1"
xyplane
edge create "edge3a3" arc radius 0.1875 startangle 0 endangle 180 center "ver3a2" xyplane
edge create "edge3a4" arc radius 0.1875 startangle 180 endangle 360 center "ver3a2"
xyplane
edge create "edge3a5" straight "ver3a3" "ver3a5"
edge create "edge3a6" straight "ver3a4" "ver3a6"
face create "h3abaface" wireframe "edge3a1" "edge3a2" real
face create "h3afface" wireframe "edge3a3" "edge3a4" real
face create "h3atface" wireframe "edge3a1" "edge3a3" "edge3a5" "edge3a6" real
face create "h3abface" wireframe "edge3a2" "edge3a4" "edge3a5" "edge3a6" real
volume create "heater3a" stitch "h3abaface" "h3afface" "h3atface" "h3abface"

vertex create "ver3b1" coordinates 16.6875  -0.0625 0
vertex create "ver3b2" coordinates 16.6875  -0.0625 8.125
vertex create "ver3b3" coordinates 16.875 -0.0625 0
vertex create "ver3b4" coordinates 16.5 -0.0625 0
vertex create "ver3b5" coordinates 16.875 -0.0625 8.125
vertex create "ver3b6" coordinates 16.5 -0.0625 8.125
edge create "edge3b1" arc radius 0.1875 startangle 0 endangle 180 center "ver3b1" xyplane
edge create "edge3b2" arc radius 0.1875 startangle 180 endangle 360 center "ver3b1"
xyplane
edge create "edge3b3" arc radius 0.1875 startangle 0 endangle 180 center "ver3b2" xyplane
edge create "edge3b4" arc radius 0.1875 startangle 180 endangle 360 center "ver3b2"
xyplane
edge create "edge3b5" straight "ver3b3" "ver3b5"
edge create "edge3b6" straight "ver3b4" "ver3b6"
face create "h3bbaface" wireframe "edge3b1" "edge3b2" real
face create "h3bfface" wireframe "edge3b3" "edge3b4" real
face create "h3btface" wireframe "edge3b1" "edge3b3" "edge3b5" "edge3b6" real
face create "h3bbface" wireframe "edge3b2" "edge3b4" "edge3b5" "edge3b6" real
volume create "heater3b" stitch "h3bbaface" "h3bfface" "h3btface" "h3bbface"

vertex create "ver3c1" coordinates 16.6875  -1.4375 0
vertex create "ver3c2" coordinates 16.6875  -1.4375 8.125
vertex create "ver3c3" coordinates 16.875 -1.4375 0
vertex create "ver3c4" coordinates 16.5 -1.4375 0
vertex create "ver3c5" coordinates 16.875 -1.4375 8.125
vertex create "ver3c6" coordinates 16.5 -1.4375 8.125
edge create "edge3c1" arc radius 0.1875 startangle 0 endangle 180 center "ver3c1" xyplane
```

```
edge create "edge3c2" arc radius 0.1875 startangle 180 endangle 360 center "ver3c1"
xyplane
edge create "edge3c3" arc radius 0.1875 startangle 0 endangle 180 center "ver3c2" xyplane
edge create "edge3c4" arc radius 0.1875 startangle 180 endangle 360 center "ver3c2"
xyplane
edge create "edge3c5" straight "ver3c3" "ver3c5"
edge create "edge3c6" straight "ver3c4" "ver3c6"
face create "h3cbaface" wireframe "edge3c1" "edge3c2" real
face create "h3cfface" wireframe "edge3c3" "edge3c4" real
face create "h3ctface" wireframe "edge3c1" "edge3c3" "edge3c5" "edge3c6" real
face create "h3cbface" wireframe "edge3c2" "edge3c4" "edge3c5" "edge3c6" real
volume create "heater3c" stitch "h3cbaface" "h3cfface" "h3ctface" "h3cbface"

vertex create "ver3d1" coordinates 16.6875  -2.8125 0
vertex create "ver3d2" coordinates 16.6875  -2.8125 8.125
vertex create "ver3d3" coordinates 16.875 -2.8125 0
vertex create "ver3d4" coordinates 16.5 -2.8125 0
vertex create "ver3d5" coordinates 16.875 -2.8125 8.125
vertex create "ver3d6" coordinates 16.5 -2.8125 8.125
edge create "edge3d1" arc radius 0.1875 startangle 0 endangle 180 center "ver3d1" xyplane
edge create "edge3d2" arc radius 0.1875 startangle 180 endangle 360 center "ver3d1"
xyplane
edge create "edge3d3" arc radius 0.1875 startangle 0 endangle 180 center "ver3d2" xyplane
edge create "edge3d4" arc radius 0.1875 startangle 180 endangle 360 center "ver3d2"
xyplane
edge create "edge3d5" straight "ver3d3" "ver3d5"
edge create "edge3d6" straight "ver3d4" "ver3d6"
face create "h3dbaface" wireframe "edge3d1" "edge3d2" real
face create "h3dfface" wireframe "edge3d3" "edge3d4" real
face create "h3dtface" wireframe "edge3d1" "edge3d3" "edge3d5" "edge3d6" real
face create "h3dbface" wireframe "edge3d2" "edge3d4" "edge3d5" "edge3d6" real
volume create "heater3d" stitch "h3dbaface" "h3dfface" "h3dtface" "h3dbface"

/heater 4
vertex create "ver4a1" coordinates 17.1875 0.3125 0
vertex create "ver4a2" coordinates 17.1875 0.3125 8.125
vertex create "ver4a3" coordinates 17.375 0.3125 0
vertex create "ver4a4" coordinates 17 0.3125 0
vertex create "ver4a5" coordinates 17.375 0.3125 8.125
vertex create "ver4a6" coordinates 17 0.3125 8.125
edge create "edge4a1" arc radius 0.1875 startangle 0 endangle 180 center "ver4a1" xyplane
edge create "edge4a2" arc radius 0.1875 startangle 180 endangle 360 center "ver4a1"
xyplane
edge create "edge4a3" arc radius 0.1875 startangle 0 endangle 180 center "ver4a2" xyplane
edge create "edge4a4" arc radius 0.1875 startangle 180 endangle 360 center "ver4a2"
xyplane
edge create "edge4a5" straight "ver4a3" "ver4a5"
edge create "edge4a6" straight "ver4a4" "ver4a6"
face create "h4abaface" wireframe "edge4a1" "edge4a2" real
face create "h4afface" wireframe "edge4a3" "edge4a4" real
face create "h4atface" wireframe "edge4a1" "edge4a3" "edge4a5" "edge4a6" real
face create "h4abface" wireframe "edge4a2" "edge4a4" "edge4a5" "edge4a6" real
volume create "heater4a" stitch "h4abaface" "h4afface" "h4atface" "h4abface"

vertex create "ver4b1" coordinates 17.1875 -1.0625 0
vertex create "ver4b2" coordinates 17.1875 -1.0625 8.125
vertex create "ver4b3" coordinates 17.375 -1.0625 0
vertex create "ver4b4" coordinates 17 -1.0625 0
vertex create "ver4b5" coordinates 17.375 -1.0625 8.125
vertex create "ver4b6" coordinates 17 -1.0625 8.125
edge create "edge4b1" arc radius 0.1875 startangle 0 endangle 180 center "ver4b1" xyplane
edge create "edge4b2" arc radius 0.1875 startangle 180 endangle 360 center "ver4b1"
xyplane
edge create "edge4b3" arc radius 0.1875 startangle 0 endangle 180 center "ver4b2" xyplane
edge create "edge4b4" arc radius 0.1875 startangle 180 endangle 360 center "ver4b2"
xyplane
edge create "edge4b5" straight "ver4b3" "ver4b5"
edge create "edge4b6" straight "ver4b4" "ver4b6"
face create "h4bbaface" wireframe "edge4b1" "edge4b2" real
face create "h4bfface" wireframe "edge4b3" "edge4b4" real
face create "h4btface" wireframe "edge4b1" "edge4b3" "edge4b5" "edge4b6" real
```

```
face create "h4bbface" wireframe "edge4b2" "edge4b4" "edge4b5" "edge4b6" real
volume create "heater4b" stitch "h4bbaface" "h4bfface" "h4btface" "h4bbface"

vertex create "ver4c1" coordinates 17.1875 -2.4375 0
vertex create "ver4c2" coordinates 17.1875 -2.4375 8.125
vertex create "ver4c3" coordinates 17.375 -2.4375 0
vertex create "ver4c4" coordinates 17 -2.4375 0
vertex create "ver4c5" coordinates 17.375 -2.4375 8.125
vertex create "ver4c6" coordinates 17 -2.4375 8.125
edge create "edge4c1" arc radius 0.1875 startangle 0 endangle 180 center "ver4c1" xyplane
edge create "edge4c2" arc radius 0.1875 startangle 180 endangle 360 center "ver4c1"
xyplane
edge create "edge4c3" arc radius 0.1875 startangle 0 endangle 180 center "ver4c2" xyplane
edge create "edge4c4" arc radius 0.1875 startangle 180 endangle 360 center "ver4c2"
xyplane
edge create "edge4c5" straight "ver4c3" "ver4c5"
edge create "edge4c6" straight "ver4c4" "ver4c6"
face create "h4cbaface" wireframe "edge4c1" "edge4c2" real
face create "h4cfface" wireframe "edge4c3" "edge4c4" real
face create "h4ctface" wireframe "edge4c1" "edge4c3" "edge4c5" "edge4c6" real
face create "h4cbface" wireframe "edge4c2" "edge4c4" "edge4c5" "edge4c6" real
volume create "heater4c" stitch "h4cbaface" "h4cfface" "h4ctface" "h4cbface"

vertex create "ver4d1" coordinates 17.1875 -3.8125 0
vertex create "ver4d2" coordinates 17.1875 -3.8125 8.125
vertex create "ver4d3" coordinates 17.375 -3.8125 0
vertex create "ver4d4" coordinates 17 -3.8125 0
vertex create "ver4d5" coordinates 17.375 -3.8125 8.125
vertex create "ver4d6" coordinates 17 -3.8125 8.125
edge create "edge4d1" arc radius 0.1875 startangle 0 endangle 180 center "ver4d1" xyplane
edge create "edge4d2" arc radius 0.1875 startangle 180 endangle 360 center "ver4d1"
xyplane
edge create "edge4d3" arc radius 0.1875 startangle 0 endangle 180 center "ver4d2" xyplane
edge create "edge4d4" arc radius 0.1875 startangle 180 endangle 360 center "ver4d2"
xyplane
edge create "edge4d5" straight "ver4d3" "ver4d5"
edge create "edge4d6" straight "ver4d4" "ver4d6"
face create "h4dbaface" wireframe "edge4d1" "edge4d2" real
face create "h4dfface" wireframe "edge4d3" "edge4d4" real
face create "h4dtface" wireframe "edge4d1" "edge4d3" "edge4d5" "edge4d6" real
face create "h4dbface" wireframe "edge4d2" "edge4d4" "edge4d5" "edge4d6" real
volume create "heater4d" stitch "h4dbaface" "h4dfface" "h4dtface" "h4dbface"

/heater5
vertex create "ver5a1" coordinates 17.6875 0.8125 0
vertex create "ver5a2" coordinates 17.6875 0.8125 8.125
vertex create "ver5a3" coordinates 17.875 0.8125 0
vertex create "ver5a4" coordinates 17.5 0.8125 0
vertex create "ver5a5" coordinates 17.875 0.8125 8.125
vertex create "ver5a6" coordinates 17.5 0.8125 8.125
edge create "edge5a1" arc radius 0.1875 startangle 0 endangle 180 center "ver5a1" xyplane
edge create "edge5a2" arc radius 0.1875 startangle 180 endangle 360 center "ver5a1"
xyplane
edge create "edge5a3" arc radius 0.1875 startangle 0 endangle 180 center "ver5a2" xyplane
edge create "edge5a4" arc radius 0.1875 startangle 180 endangle 360 center "ver5a2"
xyplane
edge create "edge5a5" straight "ver5a3" "ver5a5"
edge create "edge5a6" straight "ver5a4" "ver5a6"
face create "h5abaface" wireframe "edge5a1" "edge5a2" real
face create "h5afface" wireframe "edge5a3" "edge5a4" real
face create "h5atface" wireframe "edge5a1" "edge5a3" "edge5a5" "edge5a6" real
face create "h5abface" wireframe "edge5a2" "edge5a4" "edge5a5" "edge5a6" real
volume create "heater5a" stitch "h5abaface" "h5afface" "h5atface" "h5abface"

vertex create "ver5b1" coordinates 17.6875 -0.5625 0
vertex create "ver5b2" coordinates 17.6875 -0.5625 8.125
vertex create "ver5b3" coordinates 17.875 -0.5625 0
vertex create "ver5b4" coordinates 17.5 -0.5625 0
vertex create "ver5b5" coordinates 17.875 -0.5625 8.125
vertex create "ver5b6" coordinates 17.5 -0.5625 8.125
edge create "edge5b1" arc radius 0.1875 startangle 0 endangle 180 center "ver5b1" xyplane
```

```
edge create "edge5b2" arc radius 0.1875 startangle 180 endangle 360 center "ver5b1"
xyplane
edge create "edge5b3" arc radius 0.1875 startangle 0 endangle 180 center "ver5b2" xyplane
edge create "edge5b4" arc radius 0.1875 startangle 180 endangle 360 center "ver5b2"
xyplane
edge create "edge5b5" straight "ver5b3" "ver5b5"
edge create "edge5b6" straight "ver5b4" "ver5b6"
face create "h5bbaface" wireframe "edge5b1" "edge5b2" real
face create "h5bfface" wireframe "edge5b3" "edge5b4" real
face create "h5btface" wireframe "edge5b1" "edge5b3" "edge5b5" "edge5b6" real
face create "h5bbface" wireframe "edge5b2" "edge5b4" "edge5b5" "edge5b6" real
volume create "heater5b" stitch "h5bbaface" "h5bfface" "h5btface" "h5bbface"

vertex create "ver5c1" coordinates 17.6875 -1.9375 0
vertex create "ver5c2" coordinates 17.6875 -1.9375 8.125
vertex create "ver5c3" coordinates 17.875 -1.9375 0
vertex create "ver5c4" coordinates 17.5 -1.9375 0
vertex create "ver5c5" coordinates 17.875 -1.9375 8.125
vertex create "ver5c6" coordinates 17.5 -1.9375 8.125
edge create "edge5c1" arc radius 0.1875 startangle 0 endangle 180 center "ver5c1" xyplane
edge create "edge5c2" arc radius 0.1875 startangle 180 endangle 360 center "ver5c1"
xyplane
edge create "edge5c3" arc radius 0.1875 startangle 0 endangle 180 center "ver5c2" xyplane
edge create "edge5c4" arc radius 0.1875 startangle 180 endangle 360 center "ver5c2"
xyplane
edge create "edge5c5" straight "ver5c3" "ver5c5"
edge create "edge5c6" straight "ver5c4" "ver5c6"
face create "h5cbaface" wireframe "edge5c1" "edge5c2" real
face create "h5cfface" wireframe "edge5c3" "edge5c4" real
face create "h5ctface" wireframe "edge5c1" "edge5c3" "edge5c5" "edge5c6" real
face create "h5cbface" wireframe "edge5c2" "edge5c4" "edge5c5" "edge5c6" real
volume create "heater5c" stitch "h5cbaface" "h5cfface" "h5ctface" "h5cbface"

vertex create "ver5d1" coordinates 17.6875 -3.3125 0
vertex create "ver5d2" coordinates 17.6875 -3.3125 8.125
vertex create "ver5d3" coordinates 17.875 -3.3125 0
vertex create "ver5d4" coordinates 17.5 -3.3125 0
vertex create "ver5d5" coordinates 17.875 -3.3125 8.125
vertex create "ver5d6" coordinates 17.5 -3.3125 8.125
edge create "edge5d1" arc radius 0.1875 startangle 0 endangle 180 center "ver5d1" xyplane
edge create "edge5d2" arc radius 0.1875 startangle 180 endangle 360 center "ver5d1"
xyplane
edge create "edge5d3" arc radius 0.1875 startangle 0 endangle 180 center "ver5d2" xyplane
edge create "edge5d4" arc radius 0.1875 startangle 180 endangle 360 center "ver5d2"
xyplane
edge create "edge5d5" straight "ver5d3" "ver5d5"
edge create "edge5d6" straight "ver5d4" "ver5d6"
face create "h5dbaface" wireframe "edge5d1" "edge5d2" real
face create "h5dfface" wireframe "edge5d3" "edge5d4" real
face create "h5dtface" wireframe "edge5d1" "edge5d3" "edge5d5" "edge5d6" real
face create "h5dbface" wireframe "edge5d2" "edge5d4" "edge5d5" "edge5d6" real
volume create "heater5d" stitch "h5dbaface" "h5dfface" "h5dtface" "h5dbface"

/heater6
vertex create "ver6a1" coordinates 18.1875  1.3125 0
vertex create "ver6a2" coordinates 18.1875  1.3125 8.125
vertex create "ver6a3" coordinates 18.375 1.3125 0
vertex create "ver6a4" coordinates 18 1.3125 0
vertex create "ver6a5" coordinates 18.375 1.3125 8.125
vertex create "ver6a6" coordinates 18 1.3125 8.125
edge create "edge6a1" arc radius 0.1875 startangle 0 endangle 180 center "ver6a1" xyplane
edge create "edge6a2" arc radius 0.1875 startangle 180 endangle 360 center "ver6a1"
xyplane
edge create "edge6a3" arc radius 0.1875 startangle 0 endangle 180 center "ver6a2" xyplane
edge create "edge6a4" arc radius 0.1875 startangle 180 endangle 360 center "ver6a2"
xyplane
edge create "edge6a5" straight "ver6a3" "ver6a5"
edge create "edge6a6" straight "ver6a4" "ver6a6"
face create "h6abaface" wireframe "edge6a1" "edge6a2" real
face create "h6afface" wireframe "edge6a3" "edge6a4" real
face create "h6atface" wireframe "edge6a1" "edge6a3" "edge6a5" "edge6a6" real
```

```
face create "h6abface" wireframe "edge6a2" "edge6a4" "edge6a5" "edge6a6" real
volume create "heater6a" stitch "h6abaface" "h6afface" "h6atface" "h6abface"

vertex create "ver6b1" coordinates 18.1875  -0.0625 0
vertex create "ver6b2" coordinates 18.1875  -0.0625 8.125
vertex create "ver6b3" coordinates 18.375 -0.0625 0
vertex create "ver6b4" coordinates 18 -0.0625 0
vertex create "ver6b5" coordinates 18.375 -0.0625 8.125
vertex create "ver6b6" coordinates 18 -0.0625 8.125
edge create "edge6b1" arc radius 0.1875 startangle 0 endangle 180 center "ver6b1" xyplane
edge create "edge6b2" arc radius 0.1875 startangle 180 endangle 360 center "ver6b1"
xyplane
edge create "edge6b3" arc radius 0.1875 startangle 0 endangle 180 center "ver6b2" xyplane
edge create "edge6b4" arc radius 0.1875 startangle 180 endangle 360 center "ver6b2"
xyplane
edge create "edge6b5" straight "ver6b3" "ver6b5"
edge create "edge6b6" straight "ver6b4" "ver6b6"
face create "h6bbaface" wireframe "edge6b1" "edge6b2" real
face create "h6bfface" wireframe "edge6b3" "edge6b4" real
face create "h6btface" wireframe "edge6b1" "edge6b3" "edge6b5" "edge6b6" real
face create "h6bbface" wireframe "edge6b2" "edge6b4" "edge6b5" "edge6b6" real
volume create "heater6b" stitch "h6bbaface" "h6bfface" "h6btface" "h6bbface"

vertex create "ver6c1" coordinates 18.1875  -1.4375 0
vertex create "ver6c2" coordinates 18.1875  -1.4375 8.125
vertex create "ver6c3" coordinates 18.375 -1.4375 0
vertex create "ver6c4" coordinates 18 -1.4375 0
vertex create "ver6c5" coordinates 18.375 -1.4375 8.125
vertex create "ver6c6" coordinates 18 -1.4375 8.125
edge create "edge6c1" arc radius 0.1875 startangle 0 endangle 180 center "ver6c1" xyplane
edge create "edge6c2" arc radius 0.1875 startangle 180 endangle 360 center "ver6c1"
xyplane
edge create "edge6c3" arc radius 0.1875 startangle 0 endangle 180 center "ver6c2" xyplane
edge create "edge6c4" arc radius 0.1875 startangle 180 endangle 360 center "ver6c2"
xyplane
edge create "edge6c5" straight "ver6c3" "ver6c5"
edge create "edge6c6" straight "ver6c4" "ver6c6"
face create "h6cbaface" wireframe "edge6c1" "edge6c2" real
face create "h6cfface" wireframe "edge6c3" "edge6c4" real
face create "h6ctface" wireframe "edge6c1" "edge6c3" "edge6c5" "edge6c6" real
face create "h6cbface" wireframe "edge6c2" "edge6c4" "edge6c5" "edge6c6" real
volume create "heater6c" stitch "h6cbaface" "h6cfface" "h6ctface" "h6cbface"

vertex create "ver6d1" coordinates 18.1875  -2.8125 0
vertex create "ver6d2" coordinates 18.1875  -2.8125 8.125
vertex create "ver6d3" coordinates 18.375 -2.8125 0
vertex create "ver6d4" coordinates 18 -2.8125 0
vertex create "ver6d5" coordinates 18.375 -2.8125 8.125
vertex create "ver6d6" coordinates 18 -2.8125 8.125
edge create "edge6d1" arc radius 0.1875 startangle 0 endangle 180 center "ver6d1" xyplane
edge create "edge6d2" arc radius 0.1875 startangle 180 endangle 360 center "ver6d1"
xyplane
edge create "edge6d3" arc radius 0.1875 startangle 0 endangle 180 center "ver6d2" xyplane
edge create "edge6d4" arc radius 0.1875 startangle 180 endangle 360 center "ver6d2"
xyplane
edge create "edge6d5" straight "ver6d3" "ver6d5"
edge create "edge6d6" straight "ver6d4" "ver6d6"
face create "h6dbaface" wireframe "edge6d1" "edge6d2" real
face create "h6dfface" wireframe "edge6d3" "edge6d4" real
face create "h6dtface" wireframe "edge6d1" "edge6d3" "edge6d5" "edge6d6" real
face create "h6dbface" wireframe "edge6d2" "edge6d4" "edge6d5" "edge6d6" real
volume create "heater6d" stitch "h6dbaface" "h6dfface" "h6dtface" "h6dbface"

/heater7
vertex create "ver7a1" coordinates 18.6875 0.3125 0
vertex create "ver7a2" coordinates 18.6875 0.3125 8.125
vertex create "ver7a3" coordinates 18.875 0.3125 0
vertex create "ver7a4" coordinates 18.5 0.3125 0
vertex create "ver7a5" coordinates 18.875 0.3125 8.125
vertex create "ver7a6" coordinates 18.5 0.3125 8.125
edge create "edge7a1" arc radius 0.1875 startangle 0 endangle 180 center "ver7a1" xyplane
```

```
edge create "edge7a2" arc radius 0.1875 startangle 180 endangle 360 center "ver7a1"
xyplane
edge create "edge7a3" arc radius 0.1875 startangle 0 endangle 180 center "ver7a2" xyplane
edge create "edge7a4" arc radius 0.1875 startangle 180 endangle 360 center "ver7a2"
xyplane
edge create "edge7a5" straight "ver7a3" "ver7a5"
edge create "edge7a6" straight "ver7a4" "ver7a6"
face create "h7abaface" wireframe "edge7a1" "edge7a2" real
face create "h7afface" wireframe "edge7a3" "edge7a4" real
face create "h7atface" wireframe "edge7a1" "edge7a3" "edge7a5" "edge7a6" real
face create "h7abface" wireframe "edge7a2" "edge7a4" "edge7a5" "edge7a6" real
volume create "heater7a" stitch "h7abaface" "h7afface" "h7atface" "h7abface"

vertex create "ver7b1" coordinates 18.6875 -1.0625 0
vertex create "ver7b2" coordinates 18.6875 -1.0625 8.125
vertex create "ver7b3" coordinates 18.875 -1.0625 0
vertex create "ver7b4" coordinates 18.5 -1.0625 0
vertex create "ver7b5" coordinates 18.875 -1.0625 8.125
vertex create "ver7b6" coordinates 18.5 -1.0625 8.125
edge create "edge7b1" arc radius 0.1875 startangle 0 endangle 180 center "ver7b1" xyplane
edge create "edge7b2" arc radius 0.1875 startangle 180 endangle 360 center "ver7b1"
xyplane
edge create "edge7b3" arc radius 0.1875 startangle 0 endangle 180 center "ver7b2" xyplane
edge create "edge7b4" arc radius 0.1875 startangle 180 endangle 360 center "ver7b2"
xyplane
edge create "edge7b5" straight "ver7b3" "ver7b5"
edge create "edge7b6" straight "ver7b4" "ver7b6"
face create "h7bbaface" wireframe "edge7b1" "edge7b2" real
face create "h7bfface" wireframe "edge7b3" "edge7b4" real
face create "h7btface" wireframe "edge7b1" "edge7b3" "edge7b5" "edge7b6" real
face create "h7bbface" wireframe "edge7b2" "edge7b4" "edge7b5" "edge7b6" real
volume create "heater7b" stitch "h7bbaface" "h7bfface" "h7btface" "h7bbface"

vertex create "ver7c1" coordinates 18.6875 -2.4375 0
vertex create "ver7c2" coordinates 18.6875 -2.4375 8.125
vertex create "ver7c3" coordinates 18.875 -2.4375 0
vertex create "ver7c4" coordinates 18.5 -2.4375 0
vertex create "ver7c5" coordinates 18.875 -2.4375 8.125
vertex create "ver7c6" coordinates 18.5 -2.4375 8.125
edge create "edge7c1" arc radius 0.1875 startangle 0 endangle 180 center "ver7c1" xyplane
edge create "edge7c2" arc radius 0.1875 startangle 180 endangle 360 center "ver7c1"
xyplane
edge create "edge7c3" arc radius 0.1875 startangle 0 endangle 180 center "ver7c2" xyplane
edge create "edge7c4" arc radius 0.1875 startangle 180 endangle 360 center "ver7c2"
xyplane
edge create "edge7c5" straight "ver7c3" "ver7c5"
edge create "edge7c6" straight "ver7c4" "ver7c6"
face create "h7cbaface" wireframe "edge7c1" "edge7c2" real
face create "h7cfface" wireframe "edge7c3" "edge7c4" real
face create "h7ctface" wireframe "edge7c1" "edge7c3" "edge7c5" "edge7c6" real
face create "h7cbface" wireframe "edge7c2" "edge7c4" "edge7c5" "edge7c6" real
volume create "heater7c" stitch "h7cbaface" "h7cfface" "h7ctface" "h7cbface"

vertex create "ver7d1" coordinates 18.6875 -3.8125 0
vertex create "ver7d2" coordinates 18.6875 -3.8125 8.125
vertex create "ver7d3" coordinates 18.875 -3.8125 0
vertex create "ver7d4" coordinates 18.5 -3.8125 0
vertex create "ver7d5" coordinates 18.875 -3.8125 8.125
vertex create "ver7d6" coordinates 18.5 -3.8125 8.125
edge create "edge7d1" arc radius 0.1875 startangle 0 endangle 180 center "ver7d1" xyplane
edge create "edge7d2" arc radius 0.1875 startangle 180 endangle 360 center "ver7d1"
xyplane
edge create "edge7d3" arc radius 0.1875 startangle 0 endangle 180 center "ver7d2" xyplane
edge create "edge7d4" arc radius 0.1875 startangle 180 endangle 360 center "ver7d2"
xyplane
edge create "edge7d5" straight "ver7d3" "ver7d5"
edge create "edge7d6" straight "ver7d4" "ver7d6"
face create "h7dbaface" wireframe "edge7d1" "edge7d2" real
face create "h7dfface" wireframe "edge7d3" "edge7d4" real
face create "h7dtface" wireframe "edge7d1" "edge7d3" "edge7d5" "edge7d6" real
face create "h7dbface" wireframe "edge7d2" "edge7d4" "edge7d5" "edge7d6" real
```

```
volume create "heater7d" stitch "h7dbaface" "h7dfface" "h7dtface" "h7dbface"

/heater8
vertex create "ver8a1" coordinates 19.1875 0.8125 0
vertex create "ver8a2" coordinates 19.1875 0.8125 8.125
vertex create "ver8a3" coordinates 19.375 0.8125 0
vertex create "ver8a4" coordinates 19 0.8125 0
vertex create "ver8a5" coordinates 19.375 0.8125 8.125
vertex create "ver8a6" coordinates 19 0.8125 8.125
edge create "edge8a1" arc radius 0.1875 startangle 0 endangle 180 center "ver8a1" xyplane
edge create "edge8a2" arc radius 0.1875 startangle 180 endangle 360 center "ver8a1"
xyplane
edge create "edge8a3" arc radius 0.1875 startangle 0 endangle 180 center "ver8a2" xyplane
edge create "edge8a4" arc radius 0.1875 startangle 180 endangle 360 center "ver8a2"
xyplane
edge create "edge8a5" straight "ver8a3" "ver8a5"
edge create "edge8a6" straight "ver8a4" "ver8a6"
face create "h8abaface" wireframe "edge8a1" "edge8a2" real
face create "h8afface" wireframe "edge8a3" "edge8a4" real
face create "h8atface" wireframe "edge8a1" "edge8a3" "edge8a5" "edge8a6" real
face create "h8abface" wireframe "edge8a2" "edge8a4" "edge8a5" "edge8a6" real
volume create "heater8a" stitch "h8abaface" "h8afface" "h8atface" "h8abface"

vertex create "ver8b1" coordinates 19.1875 -0.5625 0
vertex create "ver8b2" coordinates 19.1875 -0.5625 8.125
vertex create "ver8b3" coordinates 19.375 -0.5625 0
vertex create "ver8b4" coordinates 19 -0.5625 0
vertex create "ver8b5" coordinates 19.375 -0.5625 8.125
vertex create "ver8b6" coordinates 19 -0.5625 8.125
edge create "edge8b1" arc radius 0.1875 startangle 0 endangle 180 center "ver8b1" xyplane
edge create "edge8b2" arc radius 0.1875 startangle 180 endangle 360 center "ver8b1"
xyplane
edge create "edge8b3" arc radius 0.1875 startangle 0 endangle 180 center "ver8b2" xyplane
edge create "edge8b4" arc radius 0.1875 startangle 180 endangle 360 center "ver8b2"
xyplane
edge create "edge8b5" straight "ver8b3" "ver8b5"
edge create "edge8b6" straight "ver8b4" "ver8b6"
face create "h8bbaface" wireframe "edge8b1" "edge8b2" real
face create "h8bfface" wireframe "edge8b3" "edge8b4" real
face create "h8btface" wireframe "edge8b1" "edge8b3" "edge8b5" "edge8b6" real
face create "h8bbface" wireframe "edge8b2" "edge8b4" "edge8b5" "edge8b6" real
volume create "heater8b" stitch "h8bbaface" "h8bfface" "h8btface" "h8bbface"

vertex create "ver8c1" coordinates 19.1875 -1.9375 0
vertex create "ver8c2" coordinates 19.1875 -1.9375 8.125
vertex create "ver8c3" coordinates 19.375 -1.9375 0
vertex create "ver8c4" coordinates 19 -1.9375 0
vertex create "ver8c5" coordinates 19.375 -1.9375 8.125
vertex create "ver8c6" coordinates 19 -1.9375 8.125
edge create "edge8c1" arc radius 0.1875 startangle 0 endangle 180 center "ver8c1" xyplane
edge create "edge8c2" arc radius 0.1875 startangle 180 endangle 360 center "ver8c1"
xyplane
edge create "edge8c3" arc radius 0.1875 startangle 0 endangle 180 center "ver8c2" xyplane
edge create "edge8c4" arc radius 0.1875 startangle 180 endangle 360 center "ver8c2"
xyplane
edge create "edge8c5" straight "ver8c3" "ver8c5"
edge create "edge8c6" straight "ver8c4" "ver8c6"
face create "h8cbaface" wireframe "edge8c1" "edge8c2" real
face create "h8cfface" wireframe "edge8c3" "edge8c4" real
face create "h8ctface" wireframe "edge8c1" "edge8c3" "edge8c5" "edge8c6" real
face create "h8cbface" wireframe "edge8c2" "edge8c4" "edge8c5" "edge8c6" real
volume create "heater8c" stitch "h8cbaface" "h8cfface" "h8ctface" "h8cbface"

vertex create "ver8d1" coordinates 19.1875 -3.3125 0
vertex create "ver8d2" coordinates 19.1875 -3.3125 8.125
vertex create "ver8d3" coordinates 19.375 -3.3125 0
vertex create "ver8d4" coordinates 19 -3.3125 0
vertex create "ver8d5" coordinates 19.375 -3.3125 8.125
vertex create "ver8d6" coordinates 19 -3.3125 8.125
edge create "edge8d1" arc radius 0.1875 startangle 0 endangle 180 center "ver8d1" xyplane
```

```
edge create "edge8d2" arc radius 0.1875 startangle 180 endangle 360 center "ver8d1"
xyplane
edge create "edge8d3" arc radius 0.1875 startangle 0 endangle 180 center "ver8d2" xyplane
edge create "edge8d4" arc radius 0.1875 startangle 180 endangle 360 center "ver8d2"
xyplane
edge create "edge8d5" straight "ver8d3" "ver8d5"
edge create "edge8d6" straight "ver8d4" "ver8d6"
face create "h8dbaface" wireframe "edge8d1" "edge8d2" real
face create "h8dfface" wireframe "edge8d3" "edge8d4" real
face create "h8dtface" wireframe "edge8d1" "edge8d3" "edge8d5" "edge8d6" real
face create "h8dbface" wireframe "edge8d2" "edge8d4" "edge8d5" "edge8d6" real
volume create "heater8d" stitch "h8dbaface" "h8dfface" "h8dtface" "h8dbface"

/heater9
vertex create "ver9a1" coordinates 19.6875  1.3125 0
vertex create "ver9a2" coordinates 19.6875  1.3125 8.125
vertex create "ver9a3" coordinates 19.875 1.3125 0
vertex create "ver9a4" coordinates 19.5 1.3125 0
vertex create "ver9a5" coordinates 19.875 1.3125 8.125
vertex create "ver9a6" coordinates 19.5 1.3125 8.125
edge create "edge9a1" arc radius 0.1875 startangle 0 endangle 180 center "ver9a1" xyplane
edge create "edge9a2" arc radius 0.1875 startangle 180 endangle 360 center "ver9a1"
xyplane
edge create "edge9a3" arc radius 0.1875 startangle 0 endangle 180 center "ver9a2" xyplane
edge create "edge9a4" arc radius 0.1875 startangle 180 endangle 360 center "ver9a2"
xyplane
edge create "edge9a5" straight "ver9a3" "ver9a5"
edge create "edge9a6" straight "ver9a4" "ver9a6"
face create "h9abaface" wireframe "edge9a1" "edge9a2" real
face create "h9afface" wireframe "edge9a3" "edge9a4" real
face create "h9atface" wireframe "edge9a1" "edge9a3" "edge9a5" "edge9a6" real
face create "h9abface" wireframe "edge9a2" "edge9a4" "edge9a5" "edge9a6" real
volume create "heater9a" stitch "h9abaface" "h9afface" "h9atface" "h9abface"

vertex create "ver9b1" coordinates 19.6875  -0.0625 0
vertex create "ver9b2" coordinates 19.6875  -0.0625 8.125
vertex create "ver9b3" coordinates 19.875 -0.0625 0
vertex create "ver9b4" coordinates 19.5 -0.0625 0
vertex create "ver9b5" coordinates 19.875 -0.0625 8.125
vertex create "ver9b6" coordinates 19.5 -0.0625 8.125
edge create "edge9b1" arc radius 0.1875 startangle 0 endangle 180 center "ver9b1" xyplane
edge create "edge9b2" arc radius 0.1875 startangle 180 endangle 360 center "ver9b1"
xyplane
edge create "edge9b3" arc radius 0.1875 startangle 0 endangle 180 center "ver9b2" xyplane
edge create "edge9b4" arc radius 0.1875 startangle 180 endangle 360 center "ver9b2"
xyplane
edge create "edge9b5" straight "ver9b3" "ver9b5"
edge create "edge9b6" straight "ver9b4" "ver9b6"
face create "h9bbaface" wireframe "edge9b1" "edge9b2" real
face create "h9bfface" wireframe "edge9b3" "edge9b4" real
face create "h9btface" wireframe "edge9b1" "edge9b3" "edge9b5" "edge9b6" real
face create "h9bbface" wireframe "edge9b2" "edge9b4" "edge9b5" "edge9b6" real
volume create "heater9b" stitch "h9bbaface" "h9bfface" "h9btface" "h9bbface"

vertex create "ver9c1" coordinates 19.6875  -1.4375 0
vertex create "ver9c2" coordinates 19.6875  -1.4375 8.125
vertex create "ver9c3" coordinates 19.875 -1.4375 0
vertex create "ver9c4" coordinates 19.5 -1.4375 0
vertex create "ver9c5" coordinates 19.875 -1.4375 8.125
vertex create "ver9c6" coordinates 19.5 -1.4375 8.125
edge create "edge9c1" arc radius 0.1875 startangle 0 endangle 180 center "ver9c1" xyplane
edge create "edge9c2" arc radius 0.1875 startangle 180 endangle 360 center "ver9c1"
xyplane
edge create "edge9c3" arc radius 0.1875 startangle 0 endangle 180 center "ver9c2" xyplane
edge create "edge9c4" arc radius 0.1875 startangle 180 endangle 360 center "ver9c2"
xyplane
edge create "edge9c5" straight "ver9c3" "ver9c5"
edge create "edge9c6" straight "ver9c4" "ver9c6"
face create "h9cbaface" wireframe "edge9c1" "edge9c2" real
face create "h9cfface" wireframe "edge9c3" "edge9c4" real
face create "h9ctface" wireframe "edge9c1" "edge9c3" "edge9c5" "edge9c6" real
```

```
face create "h9cbface" wireframe "edge9c2" "edge9c4" "edge9c5" "edge9c6" real
volume create "heater9c" stitch "h9cbaface" "h9cfface" "h9ctface" "h9cbface"

vertex create "ver9d1" coordinates 19.6875  -2.8125 0
vertex create "ver9d2" coordinates 19.6875  -2.8125 8.125
vertex create "ver9d3" coordinates 19.875 -2.8125 0
vertex create "ver9d4" coordinates 19.5 -2.8125 0
vertex create "ver9d5" coordinates 19.875 -2.8125 8.125
vertex create "ver9d6" coordinates 19.5 -2.8125 8.125
edge create "edge9d1" arc radius 0.1875 startangle 0 endangle 180 center "ver9d1" xyplane
edge create "edge9d2" arc radius 0.1875 startangle 180 endangle 360 center "ver9d1"
xyplane
edge create "edge9d3" arc radius 0.1875 startangle 0 endangle 180 center "ver9d2" xyplane
edge create "edge9d4" arc radius 0.1875 startangle 180 endangle 360 center "ver9d2"
xyplane
edge create "edge9d5" straight "ver9d3" "ver9d5"
edge create "edge9d6" straight "ver9d4" "ver9d6"
face create "h9dbaface" wireframe "edge9d1" "edge9d2" real
face create "h9dfface" wireframe "edge9d3" "edge9d4" real
face create "h9dtface" wireframe "edge9d1" "edge9d3" "edge9d5" "edge9d6" real
face create "h9dbface" wireframe "edge9d2" "edge9d4" "edge9d5" "edge9d6" real
volume create "heater9d" stitch "h9dbaface" "h9dfface" "h9dtface" "h9dbface"

/heater10
vertex create "ver10a1" coordinates 20.1875 0.3125 0
vertex create "ver10a2" coordinates 20.1875 0.3125 8.125
vertex create "ver10a3" coordinates 20.375 0.3125 0
vertex create "ver10a4" coordinates 20 0.3125 0
vertex create "ver10a5" coordinates 20.375 0.3125 8.125
vertex create "ver10a6" coordinates 20 0.3125 8.125
edge create "edge10a1" arc radius 0.1875 startangle 0 endangle 180 center "ver10a1"
xyplane
edge create "edge10a2" arc radius 0.1875 startangle 180 endangle 360 center "ver10a1"
xyplane
edge create "edge10a3" arc radius 0.1875 startangle 0 endangle 180 center "ver10a2"
xyplane
edge create "edge10a4" arc radius 0.1875 startangle 180 endangle 360 center "ver10a2"
xyplane
edge create "edge10a5" straight "ver10a3" "ver10a5"
edge create "edge10a6" straight "ver10a4" "ver10a6"
face create "h10abaface" wireframe "edge10a1" "edge10a2" real
face create "h10afface" wireframe "edge10a3" "edge10a4" real
face create "h10atface" wireframe "edge10a1" "edge10a3" "edge10a5" "edge10a6" real
face create "h10abface" wireframe "edge10a2" "edge10a4" "edge10a5" "edge10a6" real
volume create "heater10a" stitch "h10abaface" "h10afface" "h10atface" "h10abface"

vertex create "ver10b1" coordinates 20.1875 -1.0625 0
vertex create "ver10b2" coordinates 20.1875 -1.0625 8.125
vertex create "ver10b3" coordinates 20.375 -1.0625 0
vertex create "ver10b4" coordinates 20 -1.0625 0
vertex create "ver10b5" coordinates 20.375 -1.0625 8.125
vertex create "ver10b6" coordinates 20 -1.0625 8.125
edge create "edge10b1" arc radius 0.1875 startangle 0 endangle 180 center "ver10b1"
xyplane
edge create "edge10b2" arc radius 0.1875 startangle 180 endangle 360 center "ver10b1"
xyplane
edge create "edge10b3" arc radius 0.1875 startangle 0 endangle 180 center "ver10b2"
xyplane
edge create "edge10b4" arc radius 0.1875 startangle 180 endangle 360 center "ver10b2"
xyplane
edge create "edge10b5" straight "ver10b3" "ver10b5"
edge create "edge10b6" straight "ver10b4" "ver10b6"
face create "h10bbaface" wireframe "edge10b1" "edge10b2" real
face create "h10bfface" wireframe "edge10b3" "edge10b4" real
face create "h10btface" wireframe "edge10b1" "edge10b3" "edge10b5" "edge10b6" real
face create "h10bbface" wireframe "edge10b2" "edge10b4" "edge10b5" "edge10b6" real
volume create "heater10b" stitch "h10bbaface" "h10bfface" "h10btface" "h10bbface"

vertex create "ver10c1" coordinates 20.1875 -2.4375 0
vertex create "ver10c2" coordinates 20.1875 -2.4375 8.125
vertex create "ver10c3" coordinates 20.375 -2.4375 0
```

```
vertex create "ver10c4" coordinates 20 -2.4375 0
vertex create "ver10c5" coordinates 20.375 -2.4375 8.125
vertex create "ver10c6" coordinates 20 -2.4375 8.125
edge create "edge10c1" arc radius 0.1875 startangle 0 endangle 180 center "ver10c1"
xyplane
edge create "edge10c2" arc radius 0.1875 startangle 180 endangle 360 center "ver10c1"
xyplane
edge create "edge10c3" arc radius 0.1875 startangle 0 endangle 180 center "ver10c2"
xyplane
edge create "edge10c4" arc radius 0.1875 startangle 180 endangle 360 center "ver10c2"
xyplane
edge create "edge10c5" straight "ver10c3" "ver10c5"
edge create "edge10c6" straight "ver10c4" "ver10c6"
face create "h10cbaface" wireframe "edge10c1" "edge10c2" real
face create "h10cfface" wireframe "edge10c3" "edge10c4" real
face create "h10ctface" wireframe "edge10c1" "edge10c3" "edge10c5" "edge10c6" real
face create "h10cbface" wireframe "edge10c2" "edge10c4" "edge10c5" "edge10c6" real
volume create "heater10c" stitch "h10cbaface" "h10cfface" "h10ctface" "h10cbface"

vertex create "ver10d1" coordinates 20.1875 -3.8125 0
vertex create "ver10d2" coordinates 20.1875 -3.8125 8.125
vertex create "ver10d3" coordinates 20.375 -3.8125 0
vertex create "ver10d4" coordinates 20 -3.8125 0
vertex create "ver10d5" coordinates 20.375 -3.8125 8.125
vertex create "ver10d6" coordinates 20 -3.8125 8.125
edge create "edge10d1" arc radius 0.1875 startangle 0 endangle 180 center "ver10d1"
xyplane
edge create "edge10d2" arc radius 0.1875 startangle 180 endangle 360 center "ver10d1"
xyplane
edge create "edge10d3" arc radius 0.1875 startangle 0 endangle 180 center "ver10d2"
xyplane
edge create "edge10d4" arc radius 0.1875 startangle 180 endangle 360 center "ver10d2"
xyplane
edge create "edge10d5" straight "ver10d3" "ver10d5"
edge create "edge10d6" straight "ver10d4" "ver10d6"
face create "h10dbaface" wireframe "edge10d1" "edge10d2" real
face create "h10dfface" wireframe "edge10d3" "edge10d4" real
face create "h10dtface" wireframe "edge10d1" "edge10d3" "edge10d5" "edge10d6" real
face create "h10dbface" wireframe "edge10d2" "edge10d4" "edge10d5" "edge10d6" real
volume create "heater10d" stitch "h10dbaface" "h10dfface" "h10dtface" "h10dbface"

/heater11
vertex create "ver11a1" coordinates 20.6875 0.8125 0
vertex create "ver11a2" coordinates 20.6875 0.8125 8.125
vertex create "ver11a3" coordinates 20.875 0.8125 0
vertex create "ver11a4" coordinates 20.5 0.8125 0
vertex create "ver11a5" coordinates 20.875 0.8125 8.125
vertex create "ver11a6" coordinates 20.5 0.8125 8.125
edge create "edge11a1" arc radius 0.1875 startangle 0 endangle 180 center "ver11a1"
xyplane
edge create "edge11a2" arc radius 0.1875 startangle 180 endangle 360 center "ver11a1"
xyplane
edge create "edge11a3" arc radius 0.1875 startangle 0 endangle 180 center "ver11a2"
xyplane
edge create "edge11a4" arc radius 0.1875 startangle 180 endangle 360 center "ver11a2"
xyplane
edge create "edge11a5" straight "ver11a3" "ver11a5"
edge create "edge11a6" straight "ver11a4" "ver11a6"
face create "h11abaface" wireframe "edge11a1" "edge11a2" real
face create "h11afface" wireframe "edge11a3" "edge11a4" real
face create "h11atface" wireframe "edge11a1" "edge11a3" "edge11a5" "edge11a6" real
face create "h11abface" wireframe "edge11a2" "edge11a4" "edge11a5" "edge11a6" real
volume create "heater11a" stitch "h11abaface" "h11afface" "h11atface" "h11abface"

vertex create "ver11b1" coordinates 20.6875 -0.5625 0
vertex create "ver11b2" coordinates 20.6875 -0.5625 8.125
vertex create "ver11b3" coordinates 20.875 -0.5625 0
vertex create "ver11b4" coordinates 20.5 -0.5625 0
vertex create "ver11b5" coordinates 20.875 -0.5625 8.125
vertex create "ver11b6" coordinates 20.5 -0.5625 8.125
```

```
edge create "edge11b1" arc radius 0.1875 startangle 0 endangle 180 center "ver11b1"
xyplane
edge create "edge11b2" arc radius 0.1875 startangle 180 endangle 360 center "ver11b1"
xyplane
edge create "edge11b3" arc radius 0.1875 startangle 0 endangle 180 center "ver11b2"
xyplane
edge create "edge11b4" arc radius 0.1875 startangle 180 endangle 360 center "ver11b2"
xyplane
edge create "edge11b5" straight "ver11b3" "ver11b5"
edge create "edge11b6" straight "ver11b4" "ver11b6"
face create "h11bbaface" wireframe "edge11b1" "edge11b2" real
face create "h11bfface" wireframe "edge11b3" "edge11b4" real
face create "h11btface" wireframe "edge11b1" "edge11b3" "edge11b5" "edge11b6" real
face create "h11bbface" wireframe "edge11b2" "edge11b4" "edge11b5" "edge11b6" real
volume create "heater11b" stitch "h11bbaface" "h11bfface" "h11btface" "h11bbface"

vertex create "ver11c1" coordinates 20.6875 -1.9375 0
vertex create "ver11c2" coordinates 20.6875 -1.9375 8.125
vertex create "ver11c3" coordinates 20.875 -1.9375 0
vertex create "ver11c4" coordinates 20.5 -1.9375 0
vertex create "ver11c5" coordinates 20.875 -1.9375 8.125
vertex create "ver11c6" coordinates 20.5 -1.9375 8.125
edge create "edge11c1" arc radius 0.1875 startangle 0 endangle 180 center "ver11c1"
xyplane
edge create "edge11c2" arc radius 0.1875 startangle 180 endangle 360 center "ver11c1"
xyplane
edge create "edge11c3" arc radius 0.1875 startangle 0 endangle 180 center "ver11c2"
xyplane
edge create "edge11c4" arc radius 0.1875 startangle 180 endangle 360 center "ver11c2"
xyplane
edge create "edge11c5" straight "ver11c3" "ver11c5"
edge create "edge11c6" straight "ver11c4" "ver11c6"
face create "h11cbaface" wireframe "edge11c1" "edge11c2" real
face create "h11cfface" wireframe "edge11c3" "edge11c4" real
face create "h11ctface" wireframe "edge11c1" "edge11c3" "edge11c5" "edge11c6" real
face create "h11cbface" wireframe "edge11c2" "edge11c4" "edge11c5" "edge11c6" real
volume create "heater11c" stitch "h11cbaface" "h11cfface" "h11ctface" "h11cbface"

vertex create "ver11d1" coordinates 20.6875 -3.3125 0
vertex create "ver11d2" coordinates 20.6875 -3.3125 8.125
vertex create "ver11d3" coordinates 20.875 -3.3125 0
vertex create "ver11d4" coordinates 20.5 -3.3125 0
vertex create "ver11d5" coordinates 20.875 -3.3125 8.125
vertex create "ver11d6" coordinates 20.5 -3.3125 8.125
edge create "edge11d1" arc radius 0.1875 startangle 0 endangle 180 center "ver11d1"
xyplane
edge create "edge11d2" arc radius 0.1875 startangle 180 endangle 360 center "ver11d1"
xyplane
edge create "edge11d3" arc radius 0.1875 startangle 0 endangle 180 center "ver11d2"
xyplane
edge create "edge11d4" arc radius 0.1875 startangle 180 endangle 360 center "ver11d2"
xyplane
edge create "edge11d5" straight "ver11d3" "ver11d5"
edge create "edge11d6" straight "ver11d4" "ver11d6"
face create "h11dbaface" wireframe "edge11d1" "edge11d2" real
face create "h11dfface" wireframe "edge11d3" "edge11d4" real
face create "h11dtface" wireframe "edge11d1" "edge11d3" "edge11d5" "edge11d6" real
face create "h11dbface" wireframe "edge11d2" "edge11d4" "edge11d5" "edge11d6" real
volume create "heater11d" stitch "h11dbaface" "h11dfface" "h11dtface" "h11dbface"

/heater 12
vertex create "ver12a1" coordinates 21.1875  1.3125 0
vertex create "ver12a2" coordinates 21.1875  1.3125 8.125
vertex create "ver12a3" coordinates 21.375 1.3125 0
vertex create "ver12a4" coordinates 21 1.3125 0
vertex create "ver12a5" coordinates 21.375 1.3125 8.125
vertex create "ver12a6" coordinates 21 1.3125 8.125
edge create "edge12a1" arc radius 0.1875 startangle 0 endangle 180 center "ver12a1"
xyplane
edge create "edge12a2" arc radius 0.1875 startangle 180 endangle 360 center "ver12a1"
xyplane
```

```
edge create "edge12a3" arc radius 0.1875 startangle 0 endangle 180 center "ver12a2"
xyplane
edge create "edge12a4" arc radius 0.1875 startangle 180 endangle 360 center "ver12a2"
xyplane
edge create "edge12a5" straight "ver12a3" "ver12a5"
edge create "edge12a6" straight "ver12a4" "ver12a6"
face create "h12abaface" wireframe "edge12a1" "edge12a2" real
face create "h12afface" wireframe "edge12a3" "edge12a4" real
face create "h12atface" wireframe "edge12a1" "edge12a3" "edge12a5" "edge12a6" real
face create "h12abface" wireframe "edge12a2" "edge12a4" "edge12a5" "edge12a6" real
volume create "heater12a" stitch "h12abaface" "h12afface" "h12atface" "h12abface"

vertex create "ver12b1" coordinates 21.1875  -0.0625 0
vertex create "ver12b2" coordinates 21.1875  -0.0625 8.125
vertex create "ver12b3" coordinates 21.375 -0.0625 0
vertex create "ver12b4" coordinates 21 -0.0625 0
vertex create "ver12b5" coordinates 21.375 -0.0625 8.125
vertex create "ver12b6" coordinates 21 -0.0625 8.125
edge create "edge12b1" arc radius 0.1875 startangle 0 endangle 180 center "ver12b1"
xyplane
edge create "edge12b2" arc radius 0.1875 startangle 180 endangle 360 center "ver12b1"
xyplane
edge create "edge12b3" arc radius 0.1875 startangle 0 endangle 180 center "ver12b2"
xyplane
edge create "edge12b4" arc radius 0.1875 startangle 180 endangle 360 center "ver12b2"
xyplane
edge create "edge12b5" straight "ver12b3" "ver12b5"
edge create "edge12b6" straight "ver12b4" "ver12b6"
face create "h12bbaface" wireframe "edge12b1" "edge12b2" real
face create "h12bfface" wireframe "edge12b3" "edge12b4" real
face create "h12btface" wireframe "edge12b1" "edge12b3" "edge12b5" "edge12b6" real
face create "h12bbface" wireframe "edge12b2" "edge12b4" "edge12b5" "edge12b6" real
volume create "heater12b" stitch "h12bbaface" "h12bfface" "h12btface" "h12bbface"

vertex create "ver12c1" coordinates 21.1875  -1.4375 0
vertex create "ver12c2" coordinates 21.1875  -1.4375 8.125
vertex create "ver12c3" coordinates 21.375 -1.4375 0
vertex create "ver12c4" coordinates 21 -1.4375 0
vertex create "ver12c5" coordinates 21.375 -1.4375 8.125
vertex create "ver12c6" coordinates 21 -1.4375 8.125
edge create "edge12c1" arc radius 0.1875 startangle 0 endangle 180 center "ver12c1"
xyplane
edge create "edge12c2" arc radius 0.1875 startangle 180 endangle 360 center "ver12c1"
xyplane
edge create "edge12c3" arc radius 0.1875 startangle 0 endangle 180 center "ver12c2"
xyplane
edge create "edge12c4" arc radius 0.1875 startangle 180 endangle 360 center "ver12c2"
xyplane
edge create "edge12c5" straight "ver12c3" "ver12c5"
edge create "edge12c6" straight "ver12c4" "ver12c6"
face create "h12cbaface" wireframe "edge12c1" "edge12c2" real
face create "h12cfface" wireframe "edge12c3" "edge12c4" real
face create "h12ctface" wireframe "edge12c1" "edge12c3" "edge12c5" "edge12c6" real
face create "h12cbface" wireframe "edge12c2" "edge12c4" "edge12c5" "edge12c6" real
volume create "heater12c" stitch "h12cbaface" "h12cfface" "h12ctface" "h12cbface"

vertex create "ver12d1" coordinates 21.1875  -2.8125 0
vertex create "ver12d2" coordinates 21.1875  -2.8125 8.125
vertex create "ver12d3" coordinates 21.375 -2.8125 0
vertex create "ver12d4" coordinates 21 -2.8125 0
vertex create "ver12d5" coordinates 21.375 -2.8125 8.125
vertex create "ver12d6" coordinates 21 -2.8125 8.125
edge create "edge12d1" arc radius 0.1875 startangle 0 endangle 180 center "ver12d1"
xyplane
edge create "edge12d2" arc radius 0.1875 startangle 180 endangle 360 center "ver12d1"
xyplane
edge create "edge12d3" arc radius 0.1875 startangle 0 endangle 180 center "ver12d2"
xyplane
edge create "edge12d4" arc radius 0.1875 startangle 180 endangle 360 center "ver12d2"
xyplane
edge create "edge12d5" straight "ver12d3" "ver12d5"
```

```
edge create "edge12d6" straight "ver12d4" "ver12d6"
face create "h12dbaface" wireframe "edge12d1" "edge12d2" real
face create "h12dfface" wireframe "edge12d3" "edge12d4" real
face create "h12dtface" wireframe "edge12d1" "edge12d3" "edge12d5" "edge12d6" real
face create "h12dbface" wireframe "edge12d2" "edge12d4" "edge12d5" "edge12d6" real
volume create "heater12d" stitch "h12dbaface" "h12dfface" "h12dtface" "h12dbface"

volume create "heaterduct" stitch "hductfface" "hductlface" "hducttface" "hductboface"
"plenlface1" "plenlface2" "plenlface3"

"hductbaface"

/subtract heaters from heaterduct
volume subtract "heaterduct" volumes "heater1a" "heater1b" "heater1c" "heater1d"
"heater2a" "heater2b" "heater2c" \
"heater2d" "heater3a" "heater3b" "heater3c" "heater3d" "heater4a" "heater4b" "heater4c"
"heater4d" "heater5a" "heater5b" \
"heater5c" "heater5d" "heater6a" "heater6b" "heater6c" "heater6d" "heater7a" "heater7b"
"heater7c" "heater7d" "heater8a" \
"heater8b" "heater8c" "heater8d" "heater9a" "heater9b" "heater9c" "heater9d" "heater10a"
"heater10b" "heater10c" "heater10d"

\
"heater11a" "heater11b" "heater11c" "heater11d" "heater12a" "heater12b" "heater12c"
"heater12d"

face create "boardbaface" wireframe "edge.118" "edge.119" "edge.120" "edge.121" real
volume create "board" stitch "boardboface" "boardtface" "boardrface" "boardlface"
"boardfface" "boardbaface"

/Merge volumes
volume merge "duct1" "duct2" real
volume merge "duct1" "transition1" real
volume merge "duct1" "volume1" real
volume merge "duct1" "volume2" real
volume merge "duct1" "volume3" real
volume merge "duct1" "volume4" real
volume merge "duct1" "volume5" real
volume merge "duct1" "volume6" real
volume merge "duct1" "volume7" real
volume merge "duct1" "transition2" real

default set "MESH.TRIMESH.MAX_FACES" numeric -1
default set "MESH.TRIMESH.GRADING" numeric 6

/Meshing
face mesh "h1afface" "h1bfface" "h1cfface" "h1dfface" "h2afface" "h2bfface" "h2cfface"
"h2dfface"\
"h3afface" "h3bfface" "h3cfface" "h3dfface" "h4afface" "h4bfface" "h4cfface" "h4dfface"\
"h5afface" "h5bfface" "h5cfface" "h5dfface" "h6afface" "h6bfface" "h6cfface" "h6dfface"\
"h7afface" "h7bfface" "h7cfface" "h7dfface" "h8afface" "h8bfface" "h8cfface" "h8dfface"\
"h9afface" "h9bfface" "h9cfface" "h9dfface" "h10afface" "h10bfface" "h10cfface"
"h10dfface"\
"h11afface" "h11bfface" "h11cfface" "h11dfface" "h12afface" "h12bfface" "h12cfface"
"h12dfface" size 0.25

face mesh "h1atface" "h1btface" "h1ctface" "h1dtface" "h2atface" "h2btface" "h2ctface"
"h2dtface"\
"h3atface" "h3btface" "h3ctface" "h3dtface" "h4atface" "h4btface" "h4ctface" "h4dtface"\
"h5atface" "h5btface" "h5ctface" "h5dtface" "h6atface" "h6btface" "h6ctface" "h6dtface"\
"h7atface" "h7btface" "h7ctface" "h7dtface" "h8atface" "h8btface" "h8ctface" "h8dtface"\
"h9atface" "h9btface" "h9ctface" "h9dtface" "h10atface" "h10btface" "h10ctface"
"h10dtface"\
"h11atface" "h11btface" "h11ctface" "h11dtface" "h12atface" "h12btface" "h12ctface"
"h12dtface"\
"h1abface" "h1bbface" "h1cbface" "h1dbface" "h2abface" "h2bbface" "h2cbface" "h2dbface"\
"h3abface" "h3bbface" "h3cbface" "h3dbface" "h4abface" "h4bbface" "h4cbface" "h4dbface"\
"h5abface" "h5bbface" "h5cbface" "h5dbface" "h6abface" "h6bbface" "h6cbface" "h6dbface"\
"h7abface" "h7bbface" "h7cbface" "h7dbface" "h8abface" "h8bbface" "h8cbface" "h8dbface"\
"h9abface" "h9bbface" "h9cbface" "h9dbface" "h10abface" "h10bbface" "h10cbface"
"h10dbface"\
```

```
"h11abface"  "h11bbface"  "h11cbface"  "h11dbface"  "h12abface"  "h12bbface"  "h12cbface"
"h12dbface" size 0.25

volume mesh "heaterduct" tetrahedral size 0.25
volume mesh "plenum1" "plenum2" "plenum3" tetrahedral size 1
volume mesh "addin" tetrahedral size 1
edge mesh "edge.119" "edge127" "edge.120" "edge125" size 0.0248425
edge mesh "edge.118" "edge.121" "edge119" "edge118" size 0.25
edge mesh "edge122" "edge123" "edge121" "edge120" size 0.25
face mesh "boardboface" "boardtface" "boardlface" "boardrface" "boardfface" size 0.50
volume mesh "board" size 1
volume mesh "ovenchamber" tetrahedral size 1
volume mesh "duct1" tetrahedral size 1

/zones
solver select "Fluent 5/6"
physics create "air" ctype "FLUID" volume "ovenchamber" "plenum1" "plenum2" "plenum3"
"heaterduct" "addin"
physics create "board" ctype "SOLID" volume "board"
physics create "hductwalls" btype "WALL" face "hductfface" "hducttface" "hductboface"
physics create "intchamwall" btype "WALL" face "wallface"
physics create "oventopglass" btype "WALL" face "oventface1"
physics create "ovenfrontwall" btype "WALL" face "ovenfface1" "ovenfface2"
physics create "ovensidewall" btype "WALL" face "ovenrface" "ovenlface"
physics create "oventopwall" btype "WALL" face "oventface2"
physics create "ovenbotwall" btype "WALL" face "ovenboface1" "ovenboface2"

physics create "ductwalls" btype "WALL" face "duct1lface" "duct1rtface" "duct1fface"
"duct1boface"\
"duct2fface"  "duct2boface"  "duct2tface"  "trans1tface"  "trans1fface"  "trans1boface"
"midvane" "outervane"\
"plentface1"   "plentface2"   "plentface3"   "plenfface"   "plenboface1"   "plenboface2"
"plenboface3" "addfface"\
"addtface"   "addboface"   "trans2tface"   "trans2fface"   "trans2boface"   "elb1curbface"
"elb1curtface" "elb1curmface"\
"smstracurlface"   "smstracurrface"   "smstracurmface"   "shel1curtface"   "shel1curbface"
"shel1curmface" "horducurbface"\
"horducurtface"   "horducurmface"   "shel2curtface"   "shel2curbface"   "shel2curmface"
"elb2curbface" "elb2curtface" \
"elb2curmface" "vol6curm" "vol6curl" "vol6curr"

physics create "boardbandt" btype "WALL" face "boardboface" "boardtface"
physics create "boardleft" btype "WALL" face "boardlface"
physics create "boardrght" btype "WALL" face "boardrface"
physics create "boardfrnt" btype "WALL" face "boardfface"

physics create "heaterwalls" btype "WALL" face "h1afface" "h1atface" "h1abface"
"h1bfface" "h1btface" "h1bbface"\
"h1cfface" "h1ctface" "h1cbface" "h1dfface" "h1dtface" "h1dbface" "h2afface" "h2atface"
"h2abface" "h2bfface" \
"h2btface" "h2bbface" "h2cfface" "h2ctface" "h2cbface" "h2dfface" "h2dtface" "h2dbface"
"h3afface" "h3atface" \
"h3abface" "h3bfface" "h3btface" "h3bbface" "h3cfface" "h3ctface" "h3cbface" "h3dfface"
"h3dtface" "h3dbface"\
"h4afface" "h4atface" "h4abface" "h4bfface" "h4btface" "h4bbface" "h4cfface" "h4ctface"
"h4cbface" "h4dfface"\
"h4dtface" "h4dbface" "h5afface" "h5atface" "h5abface" "h5bfface" "h5btface" "h5bbface"
"h5cfface" "h5ctface"\
"h5cbface" "h5dfface" "h5dtface" "h5dbface" "h6afface" "h6atface" "h6abface" "h6bfface"
"h6btface" "h6bbface"\
"h6cfface" "h6ctface" "h6cbface" "h6dfface" "h6dtface" "h6dbface" "h7afface" "h7atface"
"h7abface" "h7bfface"\
"h7btface" "h7bbface" "h7cfface" "h7ctface" "h7cbface" "h7dfface" "h7dtface" "h7dbface"
"h8afface" "h8atface"\
"h8abface" "h8bfface" "h8btface" "h8bbface" "h8cfface" "h8ctface" "h8cbface" "h8dfface"
"h8dtface" "h8dbface"\
"h9afface" "h9atface" "h9abface" "h9bfface" "h9btface" "h9bbface" "h9cfface" "h9ctface"
"h9cbface" "h9dfface"\
"h9dtface"  "h9dbface"  "h10afface"  "h10atface"  "h10abface"  "h10bfface"  "h10btface"
"h10bbface" "h10cfface" "h10ctface"\
```

```
"h10cbface"  "h10dfface"  "h10dtface"  "h10dbface"  "h11afface"  "h11atface"  "h11abface"
"h11bfface" "h11btface" "h11bbface"\
"h11cfface"  "h11ctface"  "h11cbface"  "h11dfface"  "h11dtface"  "h11dbface"  "h12afface"
"h12atface" "h12abface" "h12bfface"\
"h12btface"  "h12bbface"  "h12cfface"  "h12ctface"  "h12cbface"  "h12dfface"  "h12dtface"
"h12dbface"

physics  create  "symmetryfaces"  btype  "SYMMETRY"  face  "duct1baface"  "duct2baface"
"trans1baface" "plenbaface1"\
"addbaface"  "hductbaface"  "ovenbaface"  "trans2baface"  "elb1baface"  "smstrabaface"
"shel1baface"\
"hordubaface" "shel2baface" "elb2baface" "vol6ba" "boardbaface"

physics create "fanface" btype "FAN" face "blower"

physics  create  "internalfaces"  btype  "INTERIOR"  face  "plenlface1"  "plenlface2"
"plenlface3" "plenriface1"\
"plenriface2" "plenriface3" "hductlface" "duct1tface"

export fluent5 "plusminus.msh"
```

/Author: Reinhard Powell
/This file contains the geometry and meshing for submodel geometry where heater has no fin.

```
vertex create "ver1a1" coordinates 0.75 0.85 0
vertex create "ver1a2" coordinates 0.75 0.85 0.223
vertex create "ver1a3" coordinates 0.9375 0.85 0
vertex create "ver1a4" coordinates 0.5625 0.85 0
vertex create "ver1a5" coordinates 0.9375 0.85 0.223
vertex create "ver1a6" coordinates 0.5625 0.85 0.223
edge create "edge1a1" arc radius 0.1875 startangle 0 endangle 180 center "ver1a1" xyplane
edge  create  "edge1a2"  arc  radius  0.1875  startangle  180  endangle  360  center  "ver1a1"
xyplane
edge create "edge1a3" arc radius 0.1875 startangle 0 endangle 180 center "ver1a2" xyplane
edge  create  "edge1a4"  arc  radius  0.1875  startangle  180  endangle  360  center  "ver1a2"
xyplane
edge create "edge1a5" straight "ver1a3" "ver1a5"
edge create "edge1a6" straight "ver1a4" "ver1a6"
face create "h1atface" wireframe "edge1a1" "edge1a3" "edge1a5" "edge1a6" real
face create "h1abface" wireframe "edge1a2" "edge1a4" "edge1a5" "edge1a6" real
face create "h1afface" wireframe "edge1a3" "edge1a4" real
face create "h1abaface" wireframe "edge1a1" "edge1a2" real

/heater volume
volume create "heatervol" stitch "h1atface" "h1abface" "h1afface" "h1abaface" real

/build box around heater
vertex create "ver1" coordinates 1.5  1.7 -0.4
vertex create "ver2" coordinates 1.5  1.7 0.6
vertex create "ver3" coordinates 1.5 0 -0.4
vertex create "ver4" coordinates 1.5 0 0.6
vertex create "ver5" coordinates 0 1.7 -0.4
vertex create "ver6" coordinates 0 1.7 0.6
vertex create "ver7" coordinates 0 0 -0.4
vertex create "ver8" coordinates 0 0 0.6

edge create "edge1" straight "ver6" "ver2"
edge create "edge2" straight "ver2" "ver1"
edge create "edge3" straight "ver5" "ver1"
edge create "edge4" straight "ver5" "ver6"
edge create "edge5" straight "ver8" "ver7"
edge create "edge6" straight "ver8" "ver4"
edge create "edge7" straight "ver4" "ver3"
edge create "edge8" straight "ver7" "ver3"
edge create "edge9" straight "ver1" "ver3"
edge create "edge10" straight "ver2" "ver4"
edge create "edge11" straight "ver6" "ver8"
edge create "edge12" straight "ver5" "ver7"
```

```
face create "boxtface" wireframe "edge1" "edge4" "edge3" "edge2" real
face create "boxbface" wireframe "edge7" "edge8" "edge6" "edge5" real
face create "boxfface" wireframe "edge1" "edge11" "edge10" "edge6" real
face create "boxbaface" wireframe "edge3" "edge12" "edge9" "edge8" real
face create "boxlface" wireframe "edge4" "edge12" "edge5" "edge11" real
face create "boxrface" wireframe "edge9" "edge2" "edge10" "edge7" real

volume create "box" stitch "boxtface" "boxbface" "boxlface" "boxrface" "boxfface"
"boxbaface" real

volume subtract "box" volumes "heatervol"

/ductwork
vertex create "ver10" coordinates 0 0.85 -0.4
vertex create "ver11" coordinates 0 3.4 -0.4
vertex create "ver12" coordinates 0 5.95 -0.4
vertex create "ver13" coordinates 1.5 5.95 -0.4
vertex create "ver14" coordinates 1.5 3.4 -0.4
vertex create "ver15" coordinates 1.5 0.85 -0.4

edge create "edge21" arc radius 2.55 startangle 90 endangle 270 center "ver11" xyplane
edge create "edge22" straight "ver12" "ver13"
edge create "edge23" arc radius 2.55 startangle -90 endangle 90 center "ver14" xyplane

volume create "volume1" rotate "boxlface" onedge "edge21" reverse draft 0 extended
volume create "volume3" rotate "boxrface" onedge "edge23" draft 0 extended

edge create "edge30" straight "vertex.34" "vertex.38"
edge create "edge31" straight "vertex.36" "vertex.40"
edge create "edge32" straight "vertex.37" "vertex.33"
edge create "edge33" straight "vertex.39" "vertex.35"

volume create "volume2" wireframe "edge30" "edge31" "edge32" "edge33" "edge.25" "edge.26"
"edge.24"\
"edge.29" "edge.32" "edge.37" "edge.33" "edge.34" real

/build circuit board
vertex create "ver1cb" coordinates 0.85 5.96242125984 0
vertex create "ver2cb" coordinates 0.85 5.96242125984 0.2
vertex create "ver3cb" coordinates 0.85 5.93757874016 0
vertex create "ver4cb" coordinates 0.85 5.93757874016 0.2
vertex create "ver5cb" coordinates 0.65 5.96242125984 0
vertex create "ver6cb" coordinates 0.65 5.96242125984 0.2
vertex create "ver7cb" coordinates 0.65 5.93757874016 0
vertex create "ver8cb" coordinates 0.65 5.93757874016 0.2

edge create "edge1cb" straight "ver6cb" "ver2cb"
edge create "edge2cb" straight "ver2cb" "ver1cb"
edge create "edge3cb" straight "ver5cb" "ver1cb"
edge create "edge4cb" straight "ver5cb" "ver6cb"
edge create "edge5cb" straight "ver8cb" "ver7cb"
edge create "edge6cb" straight "ver8cb" "ver4cb"
edge create "edge7cb" straight "ver4cb" "ver3cb"
edge create "edge8cb" straight "ver7cb" "ver3cb"
edge create "edge9cb" straight "ver1cb" "ver3cb"
edge create "edge10cb" straight "ver2cb" "ver4cb"
edge create "edge11cb" straight "ver6cb" "ver8cb"
edge create "edge12cb" straight "ver5cb" "ver7cb"

face create "cbtface" wireframe "edge1cb" "edge4cb" "edge3cb" "edge2cb" real
face create "cbbface" wireframe "edge7cb" "edge8cb" "edge6cb" "edge5cb" real
face create "cbfface" wireframe "edge1cb" "edge11cb" "edge10cb" "edge6cb" real
face create "cbbaface" wireframe "edge3cb" "edge12cb" "edge9cb" "edge8cb" real
face create "cblface" wireframe "edge4cb" "edge12cb" "edge5cb" "edge11cb" real
face create "cbrface" wireframe "edge9cb" "edge2cb" "edge10cb" "edge7cb" real

volume create "board" stitch "cbtface" "cbbface" "cbfface" "cbbaface" "cblface" "cbrface"
volume subtract "volume2" volumes "board"
volume create "board" stitch "cbtface" "cbbface" "cbfface" "cbbaface" "cblface" "cbrface"
```

```
edge mesh "edge9cb" "edge10cb" "edge11cb" "edge12cb" size 0.0248425
/face mesh "cbtface" "cbbface" "cbfface" "cbbaface" "cblface" "cbrface" size 0.023
volume mesh "board" size 0.05
face mesh "h1atface" "h1abface" size 0.023
volume mesh "box" "volume1" "volume2" "volume3" tetrahedral size 0.2

/zones
solver select "Fluent 5/6"
physics create "air" ctype "FLUID" volume "box" "volume1" "volume2" "volume3"
physics create "board" ctype "SOLID" volume "board"
physics create "heaterwalls" btype "WALL" face "h1atface" "h1abface"
physics create "walls" btype "WALL" face "h1afface" "h1abaface"
physics create "box_walls" btype "WALL" face "boxtface" "boxbface" "boxfface"
"boxbaface"\
"face.11" "face.12" "face.13" "face.15" "face.16" "face.17" "face.18" "face.20" "face.21"
"face.22" "face.23"\
"face.24"

physics create "boardbandt" btype "WALL" face "cbbface" "cbtface"
physics create "boardleft" btype "WALL" face "cblface"
physics create "boardrght" btype "WALL" face "cbrface"
physics create "boardfrnt" btype "WALL" face "cbfface"
physics create "boardback" btype "WALL" face "cbbaface"
physics create "fanface" btype "FAN" face "boxrface"
physics create "internalfaces" btype "INTERIOR" face "face.14" "face.19" "boxlface"

export fluent5 "fin-.msh"
```

/Author: Reinhard Powell
/This file contains the geometry and meshing for submodel geometry where heater has one fin.

```
vertex create "ver1a1" coordinates 0.75 0.85 0
vertex create "ver1a2" coordinates 0.75 0.85 0.2
vertex create "ver1a3" coordinates 0.9375 0.85 0
vertex create "ver1a4" coordinates 0.5625 0.85 0
vertex create "ver1a5" coordinates 0.9375 0.85 0.2
vertex create "ver1a6" coordinates 0.5625 0.85 0.2
edge create "edge1a1" arc radius 0.1875 startangle 0 endangle 180 center "ver1a1" xyplane
edge create "edge1a2" arc radius 0.1875 startangle 180 endangle 360 center "ver1a1"
xyplane
edge create "edge1a3" arc radius 0.1875 startangle 0 endangle 180 center "ver1a2" xyplane
edge create "edge1a4" arc radius 0.1875 startangle 180 endangle 360 center "ver1a2"
xyplane
edge create "edge1a5" straight "ver1a3" "ver1a5"
edge create "edge1a6" straight "ver1a4" "ver1a6"
face create "h1atface" wireframe "edge1a1" "edge1a3" "edge1a5" "edge1a6" real
face create "h1abface" wireframe "edge1a2" "edge1a4" "edge1a5" "edge1a6" real
face create "h1abaface" wireframe "edge1a1" "edge1a2" real

/front piece under fin
vertex create "ver2a2" coordinates 0.75 0.85 0.223
vertex create "ver2a5" coordinates 0.9375 0.85 0.223
vertex create "ver2a6" coordinates 0.5625 0.85 0.223
edge create "edge2a3" arc radius 0.1875 startangle 0 endangle 180 center "ver2a2" xyplane
edge create "edge2a4" arc radius 0.1875 startangle 180 endangle 360 center "ver2a2"
xyplane
edge create "edge2a5" straight "vertex.14" "ver2a5"
edge create "edge2a6" straight "vertex.13" "ver2a6"
face create "h2atface" wireframe "edge2a3" "edge1a3" "edge2a5" "edge2a6" real
face create "h2abface" wireframe "edge1a4" "edge2a5" "edge2a4" "edge2a6" real
face create "h2afface" wireframe "edge2a3" "edge2a4" real

/front fin
vertex create "ver2a7" coordinates 1.1469 0.85 0.223
vertex create "ver2a8" coordinates 0.3531 0.85 0.223
vertex create "ver2a9" coordinates 1.1469 0.85 0.2
vertex create "ver2a10" coordinates 0.3531 0.85 0.2
edge create "edge2a7" arc radius 0.3969 startangle 0 endangle 180 center "ver1a2" xyplane
```

```
edge create "edge2a8" arc radius 0.3969 startangle 180 endangle 360 center "ver1a2"
xyplane
edge create "edge2a9" arc radius 0.3969 startangle 0 endangle 180 center "ver2a2" xyplane
edge create "edge2a10" arc radius 0.3969 startangle 180 endangle 360 center "ver2a2"
xyplane
edge create "edge2a11" straight "ver2a9" "ver2a7"
edge create "edge2a12" straight "ver2a10" "ver2a8"
edge create "edge2a13" straight "ver2a9" "vertex.14"
edge create "edge2a14" straight "ver2a7" "ver2a5"
edge create "edge2a15" straight "vertex.20" "ver2a8"
edge create "edge2a16" straight "vertex.13" "ver2a10"
face create "fin1tface" wireframe "edge2a7" "edge2a9" "edge2a11" "edge2a12" real
face create "fin1bface" wireframe "edge2a11" "edge2a8" "edge2a10" "edge2a12" real
face create "fin1face1" wireframe "edge2a14" "edge2a5" "edge2a13" "edge2a11" real
face create "fin1face2" wireframe "edge2a15" "edge2a12" "edge2a16" "edge2a6" real
face create "fin1face3" wireframe "edge2a9" "edge2a3" "edge2a15" "edge2a14" real
face create "fin1face4" wireframe "edge2a10" "edge2a4" "edge2a15" "edge2a14" real
face create "fin1face5" wireframe "edge2a7" "edge1a3" "edge2a16" "edge2a13" real
face create "fin1face6" wireframe "edge1a4" "edge2a8" "edge2a16" "edge2a13" real

/heater volume
volume create "heatervol" stitch "h1atface" "h1abface" "h1abaface" "h2afface" "fin1face3"
"fin1face5" "fin1tface"\
"fin1bface" "fin1face4" "fin1face6" real

/build box around heater
vertex create "ver1" coordinates 1.5  1.7 -0.4
vertex create "ver2" coordinates 1.5  1.7 0.6
vertex create "ver3" coordinates 1.5 0 -0.4
vertex create "ver4" coordinates 1.5 0 0.6
vertex create "ver5" coordinates 0 1.7 -0.4
vertex create "ver6" coordinates 0 1.7 0.6
vertex create "ver7" coordinates 0 0 -0.4
vertex create "ver8" coordinates 0 0 0.6

edge create "edge1" straight "ver6" "ver2"
edge create "edge2" straight "ver2" "ver1"
edge create "edge3" straight "ver5" "ver1"
edge create "edge4" straight "ver5" "ver6"
edge create "edge5" straight "ver8" "ver7"
edge create "edge6" straight "ver8" "ver4"
edge create "edge7" straight "ver4" "ver3"
edge create "edge8" straight "ver7" "ver3"
edge create "edge9" straight "ver1" "ver3"
edge create "edge10" straight "ver2" "ver4"
edge create "edge11" straight "ver6" "ver8"
edge create "edge12" straight "ver5" "ver7"

face create "boxtface" wireframe "edge1" "edge4" "edge3" "edge2" real
face create "boxbface" wireframe "edge7" "edge8" "edge6" "edge5" real
face create "boxfface" wireframe "edge1" "edge11" "edge10" "edge6" real
face create "boxbaface" wireframe "edge3" "edge12" "edge9" "edge8" real
face create "boxlface" wireframe "edge4" "edge12" "edge5" "edge11" real
face create "boxrface" wireframe "edge9" "edge2" "edge10" "edge7" real

volume create "box" stitch "boxtface" "boxbface" "boxlface" "boxrface" "boxfface"
"boxbaface" real
volume subtract "box" volumes "heatervol"
volume create "fin1vol1" stitch "h2atface" "fin1face1" "fin1face2" "fin1face3"
"fin1face5" "fin1tface" real
volume create "fin1vol2" stitch "h2abface" "fin1face1" "fin1face2" "fin1face4"
"fin1face6" "fin1bface" real

/ductwork
vertex create "ver10" coordinates 0 0.85 -0.4
vertex create "ver11" coordinates 0 3.4 -0.4
vertex create "ver12" coordinates 0 5.95 -0.4
vertex create "ver13" coordinates 1.5 5.95 -0.4
vertex create "ver14" coordinates 1.5 3.4 -0.4
vertex create "ver15" coordinates 1.5 0.85 -0.4
```

```
edge create "edge21" arc radius 2.55 startangle 90 endangle 270 center "ver11" xyplane
edge create "edge22" straight "ver12" "ver13"
edge create "edge23" arc radius 2.55 startangle -90 endangle 90 center "ver14" xyplane

volume create "volume1" rotate "boxlface" onedge "edge21" reverse draft 0 extended
volume create "volume3" rotate "boxrface" onedge "edge23" draft 0 extended

edge create "edge30" straight "vertex.63" "vertex.59"
edge create "edge31" straight "vertex.61" "vertex.65"
edge create "edge32" straight "vertex.58" "vertex.62"
edge create "edge33" straight "vertex.60" "vertex.64"

volume create "volume2" wireframe "edge30" "edge31" "edge32" "edge33" "edge.61" "edge.56"
"edge.57" "edge.58" "edge.50" "edge.49" "edge.53" "edge.48" real

/build circuit board
vertex create "ver1cb" coordinates 0.85 5.96242125984 0
vertex create "ver2cb" coordinates 0.85 5.96242125984 0.2
vertex create "ver3cb" coordinates 0.85 5.93757874016 0
vertex create "ver4cb" coordinates 0.85 5.93757874016 0.2
vertex create "ver5cb" coordinates 0.65 5.96242125984 0
vertex create "ver6cb" coordinates 0.65 5.96242125984 0.2
vertex create "ver7cb" coordinates 0.65 5.93757874016 0
vertex create "ver8cb" coordinates 0.65 5.93757874016 0.2

edge create "edge1cb" straight "ver6cb" "ver2cb"
edge create "edge2cb" straight "ver2cb" "ver1cb"
edge create "edge3cb" straight "ver5cb" "ver1cb"
edge create "edge4cb" straight "ver5cb" "ver6cb"
edge create "edge5cb" straight "ver8cb" "ver7cb"
edge create "edge6cb" straight "ver8cb" "ver4cb"
edge create "edge7cb" straight "ver4cb" "ver3cb"
edge create "edge8cb" straight "ver7cb" "ver3cb"
edge create "edge9cb" straight "ver1cb" "ver3cb"
edge create "edge10cb" straight "ver2cb" "ver4cb"
edge create "edge11cb" straight "ver6cb" "ver8cb"
edge create "edge12cb" straight "ver5cb" "ver7cb"

face create "cbtface" wireframe "edge1cb" "edge4cb" "edge3cb" "edge2cb" real
face create "cbbface" wireframe "edge7cb" "edge8cb" "edge6cb" "edge5cb" real
face create "cbfface" wireframe "edge1cb" "edge11cb" "edge10cb" "edge6cb" real
face create "cbbaface" wireframe "edge3cb" "edge12cb" "edge9cb" "edge8cb" real
face create "cblface" wireframe "edge4cb" "edge12cb" "edge5cb" "edge11cb" real
face create "cbrface" wireframe "edge9cb" "edge2cb" "edge10cb" "edge7cb" real

volume create "board" stitch "cbtface" "cbbface" "cbfface" "cbbaface" "cblface" "cbrface"
volume subtract "volume2" volumes "board"
volume create "board" stitch "cbtface" "cbbface" "cbfface" "cbbaface" "cblface" "cbrface"

edge mesh "edge9cb" "edge10cb" "edge11cb" "edge12cb" size 0.0248425
/face mesh "cbtface" "cbbface" "cbfface" "cbbaface" "cblface" "cbrface" size 0.023
volume mesh "board" size 0.05
face mesh "h1atface" "h1abface" size 0.023
volume mesh "fin1vol1" "fin1vol2" tetrahedral size 0.023
volume mesh "box" "volume1" "volume2" "volume3" tetrahedral size 0.2

/zones
solver select "Fluent 5/6"
physics create "air" ctype "FLUID" volume "box" "volume1" "volume2" "volume3"
physics create "board" ctype "SOLID" volume "board"
physics create "fins" ctype "SOLID" volume "fin1vol1" "fin1vol2"
physics create "heaterwalls" btype "WALL" face "h1atface" "h1abface" "h2atface"
"h2abface"
physics create "walls" btype "WALL" face "h2afface" "h1abaface"
physics create "box_walls" btype "WALL" face "boxtface" "boxbface" "boxfface"
"boxbaface"\
"face.21" "face.22" "face.23" "face.25" "face.26" "face.27" "face.28" "face.30" "face.31"
"face.32" "face.33"\
"face.34"
physics create "finfaces" btype "WALL" face "fin1face3" "fin1face5" "fin1tface"
"fin1bface"\
```

```
"fin1face4" "fin1face6"

physics create "boardbandt" btype "WALL" face "cbbface" "cbtface"
physics create "boardleft" btype "WALL" face "cblface"
physics create "boardrght" btype "WALL" face "cbrface"
physics create "boardfrnt" btype "WALL" face "cbfface"
physics create "boardback" btype "WALL" face "cbbaface"
physics create "fanface" btype "FAN" face "boxrface"
physics create "internalfaces" btype "INTERIOR" face "face.24" "face.29" "boxlface"

export fluent5 "fin+.msh"
```

/Author: Reinhard Powell
/This file contains the geometry and meshing for submodel geometry where heater has fin modeled /by extra tubes.

```
vertex create "ver1a1" coordinates 0.5 0.3125 -0.023
vertex create "ver1a2" coordinates 0.5 0.3125 0.223
vertex create "ver1a3" coordinates 0.6875 0.3125 -0.023
vertex create "ver1a4" coordinates 0.3125 0.3125 -0.023
vertex create "ver1a5" coordinates 0.6875 0.3125 0.223
vertex create "ver1a6" coordinates 0.3125 0.3125 0.223
edge create "edge1a1" arc radius 0.1875 startangle 0 endangle 180 center "ver1a1" xyplane
edge create "edge1a2" arc radius 0.1875 startangle 180 endangle 360 center "ver1a1" xyplane
edge create "edge1a3" arc radius 0.1875 startangle 0 endangle 180 center "ver1a2" xyplane
edge create "edge1a4" arc radius 0.1875 startangle 180 endangle 360 center "ver1a2" xyplane
edge create "edge1a5" straight "ver1a3" "ver1a5"
edge create "edge1a6" straight "ver1a4" "ver1a6"
face create "h1atface" wireframe "edge1a1" "edge1a3" "edge1a5" "edge1a6" real
face create "h1abface" wireframe "edge1a2" "edge1a4" "edge1a5" "edge1a6" real
face create "h1afface" wireframe "edge1a3" "edge1a4" real
face create "h1abaface" wireframe "edge1a1" "edge1a2" real

vertex create "ver2a1" coordinates 0.5 1 -0.023
vertex create "ver2a2" coordinates 0.5 1 0.223
vertex create "ver2a3" coordinates 0.6875 1 -0.023
vertex create "ver2a4" coordinates 0.3125 1 -0.023
vertex create "ver2a5" coordinates 0.6875 1 0.223
vertex create "ver2a6" coordinates 0.3125 1 0.223
edge create "edge2a1" arc radius 0.1875 startangle 0 endangle 180 center "ver2a1" xyplane
edge create "edge2a2" arc radius 0.1875 startangle 180 endangle 360 center "ver2a1" xyplane
edge create "edge2a3" arc radius 0.1875 startangle 0 endangle 180 center "ver2a2" xyplane
edge create "edge2a4" arc radius 0.1875 startangle 180 endangle 360 center "ver2a2" xyplane
edge create "edge2a5" straight "ver2a3" "ver2a5"
edge create "edge2a6" straight "ver2a4" "ver2a6"
face create "h2atface" wireframe "edge2a1" "edge2a3" "edge2a5" "edge2a6" real
face create "h2abface" wireframe "edge2a2" "edge2a4" "edge2a5" "edge2a6" real
face create "h2afface" wireframe "edge2a3" "edge2a4" real
face create "h2abaface" wireframe "edge2a1" "edge2a2" real

vertex create "ver3a1" coordinates 1 0.65625 -0.023
vertex create "ver3a2" coordinates 1 0.65625 0.223
vertex create "ver3a3" coordinates 1.1875 0.65625 -0.023
vertex create "ver3a4" coordinates 0.8125 0.65625 -0.023
vertex create "ver3a5" coordinates 1.1875 0.65625 0.223
vertex create "ver3a6" coordinates 0.8125 0.65625 0.223
edge create "edge3a1" arc radius 0.1875 startangle 0 endangle 180 center "ver3a1" xyplane
edge create "edge3a2" arc radius 0.1875 startangle 180 endangle 360 center "ver3a1" xyplane
edge create "edge3a3" arc radius 0.1875 startangle 0 endangle 180 center "ver3a2" xyplane
edge create "edge3a4" arc radius 0.1875 startangle 180 endangle 360 center "ver3a2" xyplane
edge create "edge3a5" straight "ver3a3" "ver3a5"
edge create "edge3a6" straight "ver3a4" "ver3a6"
face create "h3atface" wireframe "edge3a1" "edge3a3" "edge3a5" "edge3a6" real
face create "h3abface" wireframe "edge3a2" "edge3a4" "edge3a5" "edge3a6" real
```

```
face create "h3afface" wireframe "edge3a3" "edge3a4" real
face create "h3abaface" wireframe "edge3a1" "edge3a2" real

vertex create "ver4a1" coordinates 1 1.34375 -0.023
vertex create "ver4a2" coordinates 1 1.34375 0.223
vertex create "ver4a3" coordinates 1.1875 1.34375 -0.023
vertex create "ver4a4" coordinates 0.8125 1.34375 -0.023
vertex create "ver4a5" coordinates 1.1875 1.34375 0.223
vertex create "ver4a6" coordinates 0.8125 1.34375 0.223
edge create "edge4a1" arc radius 0.1875 startangle 0 endangle 180 center "ver4a1" xyplane
edge create "edge4a2" arc radius 0.1875 startangle 180 endangle 360 center "ver4a1"
xyplane
edge create "edge4a3" arc radius 0.1875 startangle 0 endangle 180 center "ver4a2" xyplane
edge create "edge4a4" arc radius 0.1875 startangle 180 endangle 360 center "ver4a2"
xyplane
edge create "edge4a5" straight "ver4a3" "ver4a5"
edge create "edge4a6" straight "ver4a4" "ver4a6"
face create "h4atface" wireframe "edge4a1" "edge4a3" "edge4a5" "edge4a6" real
face create "h4abface" wireframe "edge4a2" "edge4a4" "edge4a5" "edge4a6" real
face create "h4afface" wireframe "edge4a3" "edge4a4" real
face create "h4abaface" wireframe "edge4a1" "edge4a2" real

/heater volume
volume create "heatervol1" stitch "h1atface" "h1abface" "h1afface" "h1abaface" real
volume create "heatervol2" stitch "h2atface" "h2abface" "h2afface" "h2abaface" real
volume create "heatervol3" stitch "h3atface" "h3abface" "h3afface" "h3abaface" real
volume create "heatervol4" stitch "h4atface" "h4abface" "h4afface" "h4abaface" real

/build box around heater
vertex create "ver1" coordinates 1.5  1.7 -0.4
vertex create "ver2" coordinates 1.5  1.7 0.6
vertex create "ver3" coordinates 1.5 0 -0.4
vertex create "ver4" coordinates 1.5 0 0.6
vertex create "ver5" coordinates 0 1.7 -0.4
vertex create "ver6" coordinates 0 1.7 0.6
vertex create "ver7" coordinates 0 0 -0.4
vertex create "ver8" coordinates 0 0 0.6

edge create "edge1" straight "ver6" "ver2"
edge create "edge2" straight "ver2" "ver1"
edge create "edge3" straight "ver5" "ver1"
edge create "edge4" straight "ver5" "ver6"
edge create "edge5" straight "ver8" "ver7"
edge create "edge6" straight "ver8" "ver4"
edge create "edge7" straight "ver4" "ver3"
edge create "edge8" straight "ver7" "ver3"
edge create "edge9" straight "ver1" "ver3"
edge create "edge10" straight "ver2" "ver4"
edge create "edge11" straight "ver6" "ver8"
edge create "edge12" straight "ver5" "ver7"

face create "boxtface" wireframe "edge1" "edge4" "edge3" "edge2" real
face create "boxbface" wireframe "edge7" "edge8" "edge6" "edge5" real
face create "boxfface" wireframe "edge1" "edge11" "edge10" "edge6" real
face create "boxbaface" wireframe "edge3" "edge12" "edge9" "edge8" real
face create "boxlface" wireframe "edge4" "edge12" "edge5" "edge11" real
face create "boxrface" wireframe "edge9" "edge2" "edge10" "edge7" real

volume create "box" stitch "boxtface" "boxbface" "boxlface" "boxrface" "boxfface"
"boxbaface" real
volume subtract "box" volumes "heatervol1" "heatervol2" "heatervol3" "heatervol4"

/ductwork
vertex create "ver10" coordinates 0 0.85 -0.4
vertex create "ver11" coordinates 0 3.4 -0.4
vertex create "ver12" coordinates 0 5.95 -0.4
vertex create "ver13" coordinates 1.5 5.95 -0.4
vertex create "ver14" coordinates 1.5 3.4 -0.4
vertex create "ver15" coordinates 1.5 0.85 -0.4

edge create "edge21" arc radius 2.55 startangle 90 endangle 270 center "ver11" xyplane
```

```
edge create "edge22" straight "ver12" "ver13"
edge create "edge23" arc radius 2.55 startangle -90 endangle 90 center "ver14" xyplane

volume create "volume1" rotate "boxlface" onedge "edge21" reverse draft 0 extended
volume create "volume3" rotate "boxrface" onedge "edge23" draft 0 extended

edge create "edge30" straight "vertex.80" "vertex.76"
edge create "edge31" straight "vertex.79" "vertex.75"
edge create "edge32" straight "vertex.82" "vertex.78"
edge create "edge33" straight "vertex.81" "vertex.77"

volume create "volume2" wireframe "edge30" "edge31" "edge32" "edge33" "edge.42" "edge.47"
"edge.43"\
"edge.44" "edge.55" "edge.50" "edge.51" "edge.52" real

/build circuit board
vertex create "ver1cb" coordinates 0.85 5.96242125984 0
vertex create "ver2cb" coordinates 0.85 5.96242125984 0.2
vertex create "ver3cb" coordinates 0.85 5.93757874016 0
vertex create "ver4cb" coordinates 0.85 5.93757874016 0.2
vertex create "ver5cb" coordinates 0.65 5.96242125984 0
vertex create "ver6cb" coordinates 0.65 5.96242125984 0.2
vertex create "ver7cb" coordinates 0.65 5.93757874016 0
vertex create "ver8cb" coordinates 0.65 5.93757874016 0.2

edge create "edge1cb" straight "ver6cb" "ver2cb"
edge create "edge2cb" straight "ver2cb" "ver1cb"
edge create "edge3cb" straight "ver5cb" "ver1cb"
edge create "edge4cb" straight "ver5cb" "ver6cb"
edge create "edge5cb" straight "ver8cb" "ver7cb"
edge create "edge6cb" straight "ver8cb" "ver4cb"
edge create "edge7cb" straight "ver4cb" "ver3cb"
edge create "edge8cb" straight "ver7cb" "ver3cb"
edge create "edge9cb" straight "ver1cb" "ver3cb"
edge create "edge10cb" straight "ver2cb" "ver4cb"
edge create "edge11cb" straight "ver6cb" "ver8cb"
edge create "edge12cb" straight "ver5cb" "ver7cb"

face create "cbtface" wireframe "edge1cb" "edge4cb" "edge3cb" "edge2cb" real
face create "cbbface" wireframe "edge7cb" "edge8cb" "edge6cb" "edge5cb" real
face create "cbfface" wireframe "edge1cb" "edge11cb" "edge10cb" "edge6cb" real
face create "cbbaface" wireframe "edge3cb" "edge12cb" "edge9cb" "edge8cb" real
face create "cblface" wireframe "edge4cb" "edge12cb" "edge5cb" "edge11cb" real
face create "cbrface" wireframe "edge9cb" "edge2cb" "edge10cb" "edge7cb" real

volume create "board" stitch "cbtface" "cbbface" "cbfface" "cbbaface" "cblface" "cbrface"
volume subtract "volume2" volumes "board"
volume create "board" stitch "cbtface" "cbbface" "cbfface" "cbbaface" "cblface" "cbrface"

edge mesh "edge9cb" "edge10cb" "edge11cb" "edge12cb" size 0.0248425
/face mesh "cbtface" "cbbface" "cbfface" "cbbaface" "cblface" "cbrface" size 0.023
volume mesh "board" size 0.05
face mesh "h1atface" "h1abface" "h2atface" "h2abface" "h3atface" "h3abface" "h4atface"
"h4abface" size 0.023
volume mesh "box" "volume1" "volume2" "volume3" tetrahedral size 0.2

/zones
solver select "Fluent 5/6"
physics create "air" ctype "FLUID" volume "box" "volume1" "volume2" "volume3"
physics create "board" ctype "SOLID" volume "board"
physics create "walls" btype "WALL" face "h1afface" "h1abaface" "h2afface" "h2abaface"
"h3afface" "h3abaface" "h4afface" "h4abaface"
physics create "heaterwalls" btype "WALL" face "h1atface" "h1abface" "h2atface"
"h2abface" "h3atface" "h3abface" "h4atface" "h4abface"
physics create "box_walls" btype "WALL" face "boxtface" "boxbface" "boxfface"
"boxbaface"\
"face.23" "face.24" "face.25" "face.27" "face.28" "face.29" "face.30" "face.32"
"face.33"\
"face.34" "face.35" "face.36"

physics create "boardbandt" btype "WALL" face "cbbface" "cbtface"
```

```
physics create "boardleft" btype "WALL" face "cblface"
physics create "boardrght" btype "WALL" face "cbrface"
physics create "boardfrnt" btype "WALL" face "cbfface"
physics create "boardback" btype "WALL" face "cbbaface"
physics create "fanface" btype "FAN" face "boxrface"
physics create "internalfaces" btype "INTERIOR" face "face.26" "face.31" "boxlface"

export fluent5 "finapp+.msh"
```

CFD Model Geometry and Meshing Code in GAMBIT/FLUENT

The C source code used for extracting the PWB temperatures versus time in FLUENT is shown below.

```
/Author: Reinhard Powell
/This file contains the user-defined C program for extracting the PWB temperatures versus time

#include "udf.h"
/*****************************************************************/
/* Data mining / writing                                         */
/*****************************************************************/
DEFINE_EXECUTE_AT_END(data_write)
{
FILE *fout;
Domain *domain = Get_Domain(1);
Thread *t = Lookup_Thread(domain, 15);
face_t f;

real FC[ND_ND];
fout = fopen("board_data.txt", "a");

begin_f_loop(f,t)
{
F_CENTROID(FC,f,t);
fprintf(fout,"%f\t%f\t%f\t%f\t%f\n", CURRENT_TIME, F_T(f,t), FC[0], FC[1], FC[2]);
}
end_f_loop(f,t)
fclose(fout);
}
```

APPENDIX B

MATLAB CODE FOR AUTOMATIC CHIP PACKAGE SEGMENTATION

In this appendix, the MATLAB source file for the automatic chip package detection algorithm are given.

```
function [sncoords,numsnak] = greedynew(im,chip_var,displacement)

%Reinhard Powell
%This program implements the Williams and Shah Greedy algorithm for up to two snakes that
are automatically detected. The automatic detection algorithm is developed by Reinhard
Powell.
tic;
p=1;
[row col] = size(im);
rendisp=im;
subsampi=60;  %number of intervals in i direction
subsampj=64;  %number of intervals in j direction

displacement1=EDGE(im,'canny',0.15);  %find edges in displacement image
imshow(displacement1)
figure
boxr=ceil(row/subsampi)-1;
boxc=ceil(col/subsampj)-1;
n=1;
p=1;
renvar=0;

for i=1:boxr:(row-boxr)
    for j=1:boxc:(col-boxc)
        newi=i+boxr-1;
        newj=j+boxc-1;
        avg(p,n)=mean(mean(displacement1(i:newi,j:newj)));    %subsample displacement
image
        n=n+1;
    end
    p=p+1;
    n=1;
end

maxgrad=0;
%find max gradient in subsampled image and i and j locations (chip 1)
for i=1:subsampi
    for j=1:subsampj
        tempren=avg(i,j);
        if tempren > maxgrad
            maxgrad = tempren;
            maxgi = i;
            maxgj = j;
        end
    end
end

%find i and j ranges of chip 1
[rowav,colav]=size(avg);
```

```
%Code starts to try to find the center point of the chip

suthresh=0.05*avg(maxgi,maxgj);


infvar1=1;
infvar2=1;
bigi=maxgi;
liti=maxgi;

%Traverse vertically
while (infvar1==1)|(infvar2==1)
      if avg(bigi+1,maxgj) > suthresh
            bigi=bigi+1;
      elseif avg(bigi+2,maxgj) > suthresh
            bigi=bigi+2;
      elseif avg(bigi+3,maxgj) > suthresh
            bigi=bigi+3;
      else
           infvar1=0;
      end

      if avg(liti-1,maxgj) > suthresh
           liti=liti-1;
      elseif avg(liti-2,maxgj) > suthresh
           liti=liti-2;
      elseif avg(liti-3,maxgj) > suthresh
           liti=liti-3;
      else
           infvar2=0;
      end
end

%Traverse horizontally
infvar1=1;
infvar2=1;
bigj=maxgj;
litj=maxgj;
while (infvar1==1)|(infvar2==1)
    if avg(maxgi,bigj+1) > suthresh
       bigj=bigj+1;
    elseif avg(maxgi,bigj+2) > suthresh
       bigj=bigj+2;
    elseif avg(maxgi,bigj+3) > suthresh
       bigj=bigj+3;
    else
       infvar1=0;
    end
    if avg(maxgi,litj-1) > suthresh
       litj=litj-1;
    elseif avg(maxgi,litj-2) > suthresh
       litj=litj-2;
    elseif avg(maxgi,litj-3) > suthresh
       litj=litj-3;
    else
       infvar2=0;
    end
end

if (bigi-liti)<3
     infvar1=1;
     infvar2=1;

    %Traverse vertically
    while (infvar1==1)|(infvar2==1)
        if (avg(bigi+1,litj) > suthresh)|(avg(bigi+1,bigj) > suthresh)
                bigi=bigi+1;
        elseif (avg(bigi+2,litj) > suthresh)|(avg(bigi+2,bigj) > suthresh)
                bigi=bigi+2;
        elseif (avg(bigi+3,litj) > suthresh)|(avg(bigi+2,bigj) > suthresh)
                bigi=bigi+3;
```

```
        else
               infvar1=0;
        end

        if (avg(liti-1,litj) > suthresh)|(avg(liti-1,bigj) > suthresh)
               liti=liti-1;
        elseif (avg(liti-2,litj) > suthresh)|(avg(liti-2,bigj) > suthresh)
               liti=liti-2;
        elseif (avg(liti-3,litj) > suthresh)|(avg(liti-3,bigj) > suthresh)
               liti=liti-3;
        else
               infvar2=0;
        end
    end
end

if (bigj-litj)<3
     infvar1=1;
     infvar2=1;

    %Traverse vertically
    while (infvar1==1)|(infvar2==1)
        if (avg(bigi,bigj+1) > suthresh)|(avg(liti,bigj+1) > suthresh)
                bigj=bigj+1;
        elseif (avg(bigi,bigj+2) > suthresh)|(avg(liti,bigj+2) > suthresh)
                bigj=bigj+2;
        elseif (avg(bigi,bigj+3) > suthresh)|(avg(liti,bigj+3) > suthresh)
                bigj=bigj+3;
        else
               infvar1=0;
        end

        if (avg(bigi,litj-1) > suthresh)|(avg(liti,litj-1) > suthresh)
               litj=litj-1;
        elseif (avg(bigi,litj-2) > suthresh)|(avg(liti,litj-2) > suthresh)
               litj=litj-2;
        elseif (avg(bigi,litj-3) > suthresh)|(avg(liti,litj-3) > suthresh)
               litj=litj-3;
        else
               infvar2=0;
        end
    end
end

mini=liti;
maxi=bigi;
minj=litj;
maxj=bigj;

avmini=mini;
avmaxi=maxi;
avminj=minj;
avmaxj=maxj;

if chip_var==2
    %zero out i and j ranges for chip 1
    for i=avmini:avmaxi
        for j=avminj:avmaxj
            avg(i,j)=0;
        end
    end

    maxgrad=0;

    %find max gradient in subsampled image and i and j locations (chip 2 maybe??)
    for i=1:subsampi
        for j=1:subsampj
           tempren=avg(i,j);
            if tempren > maxgrad
                maxgrad = tempren;
                maxgi = i;
```

```
            maxgj = j;
        end
    end
end

suthresh=0.05*avg(maxgi,maxgj);

infvar1=1;
infvar2=1;
bigi=maxgi;
liti=maxgi;


%Traverse vertically
while (infvar1==1)|(infvar2==1)
      if avg(bigi+1,maxgj) > suthresh
            bigi=bigi+1;
      elseif avg(bigi+2,maxgj) > suthresh
            bigi=bigi+2;
      elseif avg(bigi+3,maxgj) > suthresh
            bigi=bigi+3;
      else
           infvar1=0;
      end

      if avg(liti-1,maxgj) > suthresh
           liti=liti-1;
      elseif avg(liti-2,maxgj) > suthresh
           liti=liti-2;
      elseif avg(liti-3,maxgj) > suthresh
           liti=liti-3;
      else
           infvar2=0;
      end
end

%Traverse horizontally
infvar1=1;
infvar2=1;
bigj=maxgj;
litj=maxgj;
while (infvar1==1)|(infvar2==1)
    if avg(maxgi,bigj+1) > suthresh
       bigj=bigj+1;
    elseif avg(maxgi,bigj+2) > suthresh
       bigj=bigj+2;
    elseif avg(maxgi,bigj+3) > suthresh
       bigj=bigj+3;
    else
       infvar1=0;
    end
    if avg(maxgi,litj-1) > suthresh
       litj=litj-1;
    elseif avg(maxgi,litj-2) > suthresh
       litj=litj-2;
    elseif avg(maxgi,litj-3) > suthresh
       litj=litj-3;
    else
       infvar2=0;
    end
end


if (bigi-liti)<3
     infvar1=1;
     infvar2=1;

    %Traverse vertically
    while (infvar1==1)|(infvar2==1)
        if (avg(bigi+1,litj) > suthresh)|(avg(bigi+1,bigj) > suthresh)
                bigi=bigi+1;
```

```
            elseif (avg(bigi+2,litj) > suthresh)|(avg(bigi+2,bigj) > suthresh)
                    bigi=bigi+2;
            elseif (avg(bigi+3,litj) > suthresh)|(avg(bigi+2,bigj) > suthresh)
                    bigi=bigi+3;
            else
                   infvar1=0;
            end

            if (avg(liti-1,litj) > suthresh)|(avg(liti-1,bigj) > suthresh)
                   liti=liti-1;
            elseif (avg(liti-2,litj) > suthresh)|(avg(liti-2,bigj) > suthresh)
                   liti=liti-2;
            elseif (avg(liti-3,litj) > suthresh)|(avg(liti-3,bigj) > suthresh)
                   liti=liti-3;
            else
                   infvar2=0;
            end
         end
    end

    if (bigj-litj)<3
         infvar1=1;
         infvar2=1;

         %Traverse horizontally
         while (infvar1==1)|(infvar2==1)
            if (avg(bigi,bigj+1) > suthresh)|(avg(liti,bigj+1) > suthresh)
                    bigj=bigj+1;
            elseif (avg(bigi,bigj+2) > suthresh)|(avg(liti,bigj+2) > suthresh)
                    bigj=bigj+2;
            elseif (avg(bigi,bigj+3) > suthresh)|(avg(liti,bigj+3) > suthresh)
                    bigj=bigj+3;
            else
                   infvar1=0;

               end

            if (avg(bigi,litj-1) > suthresh)|(avg(liti,litj-1) > suthresh)
                   litj=litj-1;
            elseif (avg(bigi,litj-2) > suthresh)|(avg(liti,litj-2) > suthresh)
                   litj=litj-2;
            elseif (avg(bigi,litj-3) > suthresh)|(avg(liti,litj-3) > suthresh)
                   litj=litj-3;
            else
                   infvar2=0;
            end
       end
    end

    mini2=liti;
    maxi2=bigi;
    minj2=litj;
    maxj2=bigj;

    avmini2=mini2;
    avmaxi2=maxi2;
    avminj2=minj2;
    avmaxj2=maxj2;
    renvar=1;
end

%convert i and j ranges in subsampled image to i and j ranges in original displacement
image
mini=floor((avmini-1)*boxr);
maxi=ceil((avmaxi+0.5)*boxr);
minj=floor((avminj-1)*boxc);
maxj=ceil((avmaxj+0.5)*boxc);

if renvar==1
    mini2=floor((avmini2-1)*boxr);
    maxi2=ceil((avmaxi2+0.5)*boxr);
```

```
    minj2=floor((avminj2-1)*boxc);
    maxj2=ceil((avmaxj2+0.5)*boxc);
end

%Setup the 5 x 5 neighborhood pixels
neibc1(1:5)=2;
neibc2(1:5)=1;
neibc3(1:5)=0;
neibc4(1:5)=-1;
neibc5(1:5)=-2;
neibc6=[2 1 0 -1 -2];
neighbors(:,1)=[neibc6 neibc6 neibc6 neibc6 neibc6]';
neighbors(:,2)=[neibc1 neibc2 neibc3 neibc4 neibc5]';
neilength=25;

im=mat2gray(displacement);
numsnak=1;
clf;
hold on;
imagesc(rendisp);    %plot displacement image
axis tight
axis ij;

numpts=32;       %number of points in the snake
ndivs=numpts/4;  %number of divisions on each side
stepi=round((maxi-mini)/ndivs);
stepj=round((maxj-minj)/ndivs);

tcords1(2,:)=[mini:stepi:(mini+((ndivs-1)*stepi))];
tcords1(1,:)=minj;
tcords2(1,:)=[minj:stepj:(minj+((ndivs-1)*stepj))];
tcords2(2,:)=maxi;
tcords3(2,:)=[maxi:-stepi:(maxi-((ndivs-1)*stepi))];
tcords3(1,:)=maxj;
tcords4(1,:)=[maxj:-stepj:(maxj-((ndivs-1)*stepj))];
tcords4(2,:)=mini;
coords1=[tcords1 tcords2 tcords3 tcords4];     %coordinates of first snake
if renvar==1
    stepi2=round((maxi2-mini2)/ndivs);
    stepj2=round((maxj2-minj2)/ndivs);
    tcords1(2,:)=[mini2:stepi2:(mini2+((ndivs-1)*stepi2))];
    tcords1(1,:)=minj2;
    tcords2(1,:)=[minj2:stepj2:(minj2+((ndivs-1)*stepj2))];
    tcords2(2,:)=maxi2;
    tcords3(2,:)=[maxi2:-stepi2:(maxi2-((ndivs-1)*stepi2))];
    tcords3(1,:)=maxj2;
    tcords4(1,:)=[maxj2:-stepj2:(maxj2-((ndivs-1)*stepj2))];
    tcords4(2,:)=mini2;
    coords2=[tcords1 tcords2 tcords3 tcords4]; %coordinates id second snake
end

mov = avifile('chip2mov.avi');
mov.Quality = 100;
mov.FPS = 1;

%plot snakes
clf;
hold on;
imagesc(displacement);
axis tight
axis ij;
if renvar==0
   plot(coords1(1,:),coords1(2,:),'ro-','LineWidth',2);
   plot([coords1(1,1) coords1(1,end)],[coords1(2,1) coords1(2,end)],'ro-','LineWidth',2);
   F = getframe;
   mov = addframe(mov,F);
end


if renvar==1
    plot(coords1(1,:),coords1(2,:),'ro-','LineWidth',2);
```

```
    plot([coords1(1,1) coords1(1,end)],[coords1(2,1) coords1(2,end)],'ro-
','LineWidth',2);
    plot(coords2(1,:),coords2(2,:),'ko-','LineWidth',2);
    plot([coords2(1,1) coords2(1,end)],[coords2(2,1) coords2(2,end)],'ko-
','LineWidth',2);
    F = getframe;
    mov = addframe(mov,F);
end
drawnow;
figure;

%Rearrange image gradient file
gradim=-95*double(displacement1);
gradim = gradim - min(gradim(:));

%Set curvature threshold
curvthres = 0.3;

%Set edge threshold somewhere between the max and min image gradients
edgethres = (max(gradim(:)) - min(gradim(:)))*0.5 + min(gradim(:));

% Initialize alphas, betas and gammas
alpha(1:numpts) = 1;
beta(1:numpts) = 1.5;
gamma(1:numpts) = 8;
if renvar==1
    beta2(1:numpts)=1;
end

% Calculate the average distance
davg = 0;
davg2 = 0;
for i = 1:numpts,
               if i == numpts,
                      inext = 1;
               else
                      inext = i + 1;
               end
               davg = davg + norm(coords1(:, i) - coords1(:, inext));
        if renvar==1
            davg2 = davg2 + norm(coords2(:, i) - coords2(:, inext));
        end
end
davg = davg / (numpts);
if renvar==1
    davg2 = davg2 / (numpts);
end

% whileFlag keep the main loop going
flag = 1;
while (flag)
        % Counts the number of points which have been moved
        ptsmoved = 0;
    ptsmoved2 = 0;
        % Loop to move points to new locations
        for i = 1:numpts,
               % Modulo compensation
               if i == 1,
                      iprev = numpts;
               else
                      iprev = i - 1;
               end

               if i == numpts,
                      inext = 1;
               else
                      inext = i + 1;
               end

               % Set Emin high
               Emin = 1000000;
```

```
Emin2 = 1000000;
for q=1:neilength
              %curpt = coords1(:,i) + (neighbors(q,:))';
    curgradcoords = coords1(:,i) + (neighbors(q,:))';
    neigrads(q) = gradim(curgradcoords(2),curgradcoords(1));
    if renvar==1
        %curpt2 = coords2(:,i) + (neighbors(q,:))';
        curgradcoords2 = coords2(:,i) + (neighbors(q,:))';
        neigrads2(q) = gradim(curgradcoords2(2),curgradcoords2(1));
    end
end

       % Normalize the gradient neighborhood
       gmin = min(neigrads);
       gmax = max(neigrads);
       grange = gmax - gmin;
if renvar==1
    gmin2 = min(neigrads2);
           gmax2 = max(neigrads2);
           grange2 = gmax2 - gmin2;
end

       if grange < 5,
              grange = 5;
              gmin = gmax - 5;
       end
if renvar==1
    if grange2 < 5,
                  grange2 = 5;
                  gmin2 = gmax2 - 5;
    end
       end

neigrads = (gmin - neigrads)/(grange);
if renvar==1
    neigrads2 = (gmin2 - neigrads2)/(grange2);
end

       % Go through the neighborhood to determine next point
       for j = 1:neilength,
              curpt = coords1(:,i) + neighbors(j,:)'; % Location being considered
    if renvar==1
        curpt2 = coords2(:,i) + neighbors(j,:)'; % Location being considered
    end

              % Calculate Continuity term
              Econt(j) = abs(davg - norm(curpt - coords1(:, iprev)));
    if renvar==1
        Econt2(j) = abs(davg2 - norm(curpt2 - coords2(:, iprev)));
    end

              % Calculate curvature term
              Ecurv(j) = norm(coords1(:, iprev) - 2*curpt + coords1(:, inext))^2;
    if renvar==1
        Ecurv2(j) = norm(coords2(:, iprev) - 2*curpt2 + coords2(:, inext))^2;
    end

              % Calculate image energy term (very sensitive to this)
              Eimage(j) = -neigrads(j);
    if renvar==1
        Eimage2(j) = -neigrads2(j);
    end
       end

       % Normalize continuity and energy terms in the current neigborhood
       if (max(Econt) - min(Econt)) == 0,
              Econtrange = 1;
       else
              Econtrange = max(Econt) - min(Econt);
       end;
```

```
        if renvar==1
            if (max(Econt2) - min(Econt2)) == 0,
                        Econtrange2 = 1;
                else
                        Econtrange2 = max(Econt2) - min(Econt2);
                end;
        end

               if (max(Ecurv) - min(Ecurv)) == 0,
                       Ecurvrange = 1;
               else
                       Ecurvrange = max(Ecurv) - min(Ecurv);
               end;

        if renvar==1
            if (max(Ecurv2) - min(Ecurv2)) == 0,
                        Ecurvrange2 = 1;
                else
                        Ecurvrange2 = max(Ecurv2) - min(Ecurv2);
                end;
        end

               Econt = (Econt - min(Econt))/Econtrange;
               Ecurv = (Ecurv - min(Ecurv))/Ecurvrange;

        if renvar==1
            Econt2 = (Econt2 - min(Econt2))/Econtrange2;
                   Ecurv2 = (Ecurv2 - min(Ecurv2))/Ecurvrange2;
        end

               % Add up energies in vector form
               Et = alpha(i) * Econt + beta(i) * Ecurv + gamma(i) * Eimage;
        if renvar==1
            Et2 = alpha(i) * Econt2 + beta2(i) * Ecurv2 + gamma(i) * Eimage2;
        end

               % Determine the smallest energy in the neighborhood, save position
               % and edge magnitude
               for j = 1:neilength,
                       curpt = coords1(:,i) + neighbors(j,:)';
                       if Et(j) < Emin
                               Emin = Et(j);
                               minneipt = curpt;
                               minneigrad = gradim(curpt(2), curpt(1));
                       end
            if renvar==1
                curpt2 = coords2(:,i) + neighbors(j,:)';
                           if Et2(j) < Emin2
                                   Emin2 = Et2(j);
                                   minneipt2 = curpt2;
                                   minneigrad2 = gradim(curpt2(2), curpt2(1));
                           end
            end
        end

               % If a point is moved to a new location, increment the counter of moved
points
               if (minneipt(2) ~= coords1(2, i) & minneipt(1) ~= coords1(1, i))
                       ptsmoved = ptsmoved + 1;
               end
        if renvar==1
            if (minneipt2(2) ~= coords2(2, i) & minneipt2(1) ~= coords2(1, i))
                           ptsmoved2 = ptsmoved2 + 1;
                end
        end

               % Move the point to the new location
               coords1(:, i) = minneipt;
               edgestrength(i) = minneigrad;
        if renvar==1
            coords2(:, i) = minneipt2;
```

```
                edgestrength2(i) = minneigrad2;
    end
end

   % Figure out which corners to allow

   % Find curvatures
   for i = 1:numpts,
          if i == numpts,
                 inext = 1;
          else
                 inext = i+1;
          end

          if i== 1,
                 iprev = numpts;
          else
                 iprev = i - 1;
          end

          ui = coords1(:, i) - coords1(:, iprev);
          if ui == [ 0; 0 ], ui = [ 1 ;1 ] ; end;
          uinext = coords1(:, inext) - coords1(:, i);
          if uinext == [ 0; 0 ], uinext = [ 1 ;1 ]; end;
          curv(i) = norm(ui/norm(ui) - uinext/norm(uinext))^2;
    if renvar==1
        ui2 = coords2(:, i) - coords2(:, iprev);
              if ui2 == [ 0; 0 ], ui2 = [ 1 ;1 ] ; end;
              uinext2 = coords2(:, inext) - coords2(:, i);
              if uinext2 == [ 0; 0 ], uinext2 = [ 1 ;1 ]; end;
              curv2(i) = norm(ui2/norm(ui2) - uinext2/norm(uinext2))^2;
    end
end

   % Loosen Beta(i)
   for i = 1:numpts,
          if i == numpts,
                 inext = 1;
          else
                 inext = i+1;
          end

          if i== 1,
                 iprev = numpts;
          else
                 iprev = i - 1;
          end

          if (curv(i) > curv(iprev) & curv(i) > curv(inext) &...
                 curv(i) > curvthres & edgestrength(i) < edgethres)
                 beta(i) = 0;
          else
                 beta(i) = 1;
          end
    if renvar==1
        if (curv2(i) > curv2(iprev) & curv2(i) > curv2(inext) &...
                    curv2(i) > curvthres & edgestrength2(i) < edgethres)

                    beta2(i) = 0;
              else
                    beta2(i) = 1;
              end
    end
end

clf;
hold on;
imagesc(im);
axis tight
axis ij;
```

```
   if renvar==0
        plot(coords1(1,:),coords1(2,:),'ro-','LineWidth',2);
        plot([coords1(1,1) coords1(1,end)],[coords1(2,1) coords1(2,end)],'ro-
','LineWidth',2);
        F = getframe;
        mov = addframe(mov,F);
   end



   if renvar==1
       plot(coords1(1,:),coords1(2,:),'ro-','LineWidth',2);
       plot([coords1(1,1) coords1(1,end)],[coords1(2,1) coords1(2,end)],'ro-
','LineWidth',2);
       plot(coords2(1,:),coords2(2,:),'ko-','LineWidth',2);
       plot([coords2(1,1) coords2(1,end)],[coords2(2,1) coords2(2,end)],'ko-
','LineWidth',2);
       F = getframe;
       mov = addframe(mov,F);
   end
   drawnow;

    davg = 0;
        for i = 1:numpts,
               if i == numpts,
                      inext = 1;
               else
                      inext = i + 1;
               end;
               davg = davg + norm(coords1(:, inext) - coords1(:,i));
        end
        davg = davg / (numpts);

        % If no points are moving, break out
        if (ptsmoved < 1) & (renvar == 0),
               flag = 0;
        end

    if renvar==1
        davg2 = 0;
            for i = 1:numpts,
                   if i == numpts,
                          inext = 1;
                   else
                          inext = i + 1;
                   end;
                   davg2 = davg2 + norm(coords2(:, inext) - coords2(:,i));
            end
            davg2 = davg2 / (numpts);

            % If no points are moving, break out
            if (ptsmoved2 < 1) & (ptsmoved < 1),
                   flag = 0;
            end
    end
end
sncoords=zeros(2,numpts);
if renvar==1
    sncoords=zeros(4,numpts);
end
sncoords=coords1;
if renvar==1
    sncoords(1:2,:)=coords1;
    sncoords(3:4,:)=coords2;
    numsnak=2;
end

tdone=toc

clf;
```

```
hold on;
imagesc(displacement);
axis tight
axis ij;
if renvar==0
   plot(coords1(1,:),coords1(2,:),'ro-','LineWidth',2);
   plot([coords1(1,1) coords1(1,end)],[coords1(2,1) coords1(2,end)],'ro-','LineWidth',2);
   F = getframe;
   mov = addframe(mov,F);
end
if renvar==1
    plot(coords1(1,:),coords1(2,:),'ro-','LineWidth',2);
    plot([coords1(1,1) coords1(1,end)],[coords1(2,1) coords1(2,end)],'ro-
','LineWidth',2);
    plot(coords2(1,:),coords2(2,:),'ko-','LineWidth',2);
    plot([coords2(1,1) coords2(1,end)],[coords2(2,1) coords2(2,end)],'ko-
','LineWidth',2);
    F = getframe;
    mov = addframe(mov,F);
end

mov = close(mov);
```

APPENDIX C

ANSYS CODE AND MATERIAL PROPERTIES

C.1 FR-4 Material Properties

The material properties for FR-4 are shown in Table C.1 [79].

Table C.1. FR-4 Temperature dependent material properties

Temperature (K)	**303**	**368**	**383**	**398**	**423**	**543**
Young's Modulus, E_x (GPa)	22.4	20.7	20.0	19.3	17.9	16.0
Young's Modulus, E_y (GPa)	22.4	20.7	20.0	19.3	17.9	16.0
Young's Modulus, E_z (GPa)	1.6	1.2	1.1	1.0	0.6	0.5
Poisson's Ratio, ν_{xy}	0.136	0.136	0.136	0.136	0.136	0.136
Poisson's Ratio, ν_{xz}	0.143	0.143	0.143	0.143	0.143	0.143
Poisson's Ratio, ν_{yz}	0.143	0.143	0.143	0.143	0.143	0.143
Coefficient of Thermal Expansion, CTE_x (ppm/K)	20.0	20.0	20.0	20.0	20.0	20.0
Coefficient of Thermal Expansion, CTE_y (ppm/K)	20.0	20.0	20.0	20.0	20.0	20.0
Coefficient of Thermal Expansion, CTE_z (ppm/K)	86.5	86.5	243.0	400.0	400.0	400.0
Shear Modulus, G_{xy} (GPa)	630	600	550	500	450	441
Shear Modulus, G_{xz} (GPa)	199	189	173	157	142	139.3
Shear Modulus, G_{yz} (GPa)	199	189	173	157	142	139.3

C.2 ANSYS APDL Code

In this appendix, the APDL code used for the FE model is listed.

File: pwbgeo.txt (Main input file)

```
FINISH
/CLEAR,NOSTART
/COLOR,PBAK,OFF
/PREP7

incc=1e-3
/INPUT,'mat_props','txt','C:\Documents and Settings\Reinhard Powell\Desktop\FEA_RP',, 0
/INPUT,'elements','txt','C:\Documents and Settings\Reinhard
Powell\Desktop\FEA_RP',, 0

!Build PWB Geometry

!PWB
```

```
pwb_len = 203.2      ! PWB length in x direction: 8"
pwb_wid = 139.7      ! PWB  width in y direction: 5.5"

pwb_nls = 7             ! PWB number of layers
*DIM,pwb_hls,ARRAY,pwb_nls

pwb_het = 0.631      ! PWB height in z direction: 0.0248"
pwb_hls(1) = 0.018,0.127,0.018,0.305,0.018,0.127,0.018

!  assign real constants

R,sh91                                  ! real constants for shell91
RMODIF,sh91,1   ,pwb_nls                ! 7 layers
RMODIF,sh91,19  ,mat_pwf,0,pwb_hls(2)      ! 2nd layer: FR-4
RMODIF,sh91,25  ,mat_pwc,0,pwb_hls(3)      ! 3rd layer: copper
RMODIF,sh91,31  ,mat_pwf,0,pwb_hls(4)      ! 4th layer: FR-4
RMODIF,sh91,37  ,mat_pwc,0,pwb_hls(5)      ! 5th layer: copper
RMODIF,sh91,43  ,mat_pwf,0,pwb_hls(6)      ! 6th layer: FR-4
RMODIF,sh91,13  ,mat_pwc,0,pwb_hls(1)    !   1st layer: copper trace
RMODIF,sh91,49  ,mat_pwc,0,pwb_hls(7)    !   7th layer: copper trace

rail_thk=3


NUMCMP,KP
KSEL,ALL
*GET,ar30,KP,0,NUM,MAX                  ! get current max KP number
K,ar30+1, pwb_len/2-rail_thk, pwb_wid/2,0              ! build keypoints
K,ar30+2,-pwb_len/2+rail_thk, pwb_wid/2,0
K,ar30+3,-pwb_len/2+rail_thk,-pwb_wid/2,0
K,ar30+4, pwb_len/2-rail_thk,-pwb_wid/2,0
K,ar30+5, pwb_len/2, pwb_wid/2,0              ! build keypoints
K,ar30+6,-pwb_len/2, pwb_wid/2,0
K,ar30+7,-pwb_len/2,-pwb_wid/2,0
K,ar30+8, pwb_len/2,-pwb_wid/2,0

L,ar30+1,ar30+2,                        ! build lines
L,ar30+2,ar30+3,20
L,ar30+3,ar30+4,
L,ar30+4,ar30+1,20
L,ar30+5,ar30+1,2                        ! build lines
L,ar30+2,ar30+6,2
L,ar30+6,ar30+7,20
L,ar30+7,ar30+3,2
L,ar30+4,ar30+8,2
L,ar30+8,ar30+5,20

A,ar30+2,ar30+3,ar30+7,ar30+6           ! build area
pwb_ar1=_RETURN                         ! area number
A,ar30+2,ar30+1,ar30+4,ar30+3           ! build area
pwb_ar2=_RETURN                         ! area number
A,ar30+1,ar30+5,ar30+8,ar30+4           ! build area
pwb_ar3=_RETURN                         ! area number

!*****************************************************************

!1st PBGA
!Move coodinate system to BGA location
bgaxloc=60
bgayloc=-30

ar30=100                                 ! temporary CS number
CLOCAL,ar30,0  ,bgaxloc,bgayloc,0

!BGA geometry
/INPUT,'BGA_352_eff_sil','txt','C:\Documents and Settings\Reinhard
Powell\Desktop\FEA_RP',,


ar30=100                                 ! temporary CS number
```

```
CLOCAL,ar30,0  ,-bgaxloc,-bgayloc,0


!Overlap PWB with bottom of balls
ALLSEL,ALL
ASEL,S,LOC,X,-pwb_len/2+rail_thk,pwb_len/2-rail_thk
ASEL,R,LOC,Y,-pwb_wid/2, pwb_wid/2
ASEL,R,LOC,Z,0,0
AOVLAP,ALL

!Mesh 1st PBGA
!Move coodinate system to BGA location
bgaxloc=60
bgayloc=-30

ar30=100                                ! temporary CS number
CLOCAL,ar30,0  ,bgaxloc,bgayloc,0

!BGA mesh
/INPUT,'BGA_352_msh_eff_sil1','txt','C:\Documents and Settings\Reinhard
Powell\Desktop\FEA_RP',,

ar30=100                                ! temporary CS number
CLOCAL,ar30,0  ,-bgaxloc,-bgayloc,0

!Mesh PWB
KEYOPT,sh91,11,1
ASEL,S,LOC,X,(pwb_len/2)-rail_thk,pwb_len/2
ASEL,R,LOC,Y,-pwb_wid/2, pwb_wid/2
ASEL,R,LOC,Z,-incc,incc
CM,nvl_bgs3,AREA
AATT,-1,sh91,sh91
MSHKEY,1
MSHAPE,0,2D
AMESH,nvl_bgs3

ASEL,S,LOC,X,-pwb_len/2,-(pwb_len/2)+rail_thk
ASEL,R,LOC,Y,-pwb_wid/2, pwb_wid/2
ASEL,R,LOC,Z,-incc,incc
CM,nvl_bgs4,AREA
AATT,-1,sh91,sh91
MSHKEY,1
MSHAPE,0,2D
AMESH,nvl_bgs4

ASEL,S,LOC,X,-pwb_len/2+rail_thk,(pwb_len/2)-rail_thk
ASEL,R,LOC,Y,-pwb_wid/2, pwb_wid/2
ASEL,R,LOC,Z,-incc,incc
CM,nvl_bgs4,AREA
AATT,-1,sh91,sh91
MSHKEY,0
MSHAPE,1,2D
ESIZE,10
AMESH,nvl_bgs4


!/INPUT,'conandload','txt','C:\Documents and Settings\Reinhard Powell\Desktop\FEA_RP',,
!/INPUT,'postproc','txt','C:\Documents and Settings\Reinhard Powell\Desktop\FEA_RP',,
```

File: matprops.txt (Material Properties)

```
!-------------------------------------------------------------------------------
!  material numbers

mat_pwf = 1                             ! PWB FR-4
mat_pwc = 2                             ! PWB copper

mat_bgs = 3                             ! BGA substrate
mat_bgm = 4                             ! BGA molding
mat_bgb = 5                             ! BGA solder ball
mat_sil = 6                             ! BGA silicon
```

```
MP,EX  ,mat_bgs,14000                ! BGA substrate
MP,PRXY,mat_bgs,0.15
MP,ALPX,mat_bgs,15e-6
MP,DENS,mat_bgs,3.0e-6

MP,EX  ,mat_bgm,15000                ! BGA molding
MP,PRXY,mat_bgm,0.15
MP,ALPX,mat_bgm,17.5e-6
MP,DENS,mat_bgm,3.0e-6

MP,EX  ,mat_bgb,30000                ! BGA solder ball
MP,PRXY,mat_bgb,0.31
MP,ALPX,mat_bgb,24.7e-6
MP,DENS,mat_bgb,4.5e-6

MP,EX  ,mat_pwc,79510                ! PWB copper
MP,PRXY,mat_pwc,0.32
MP,ALPX,mat_pwc,18.94e-6
MP,DENS,mat_pwc,8.94e-6

! Silicon

UIMP,mat_sil,ALPX,ALPY,ALPZ,2.6E-6,2.6E-6,2.6E-6
UIMP,mat_sil,EX,EY,EZ,1.6E5,1.6E5,1.6E5
UIMP,mat_sil,GXZ,GXY,GYZ,6.5E4,6.5E4,6.5E4
UIMP,mat_sil,NUXZ,NUXY,NUYZ,0.23,0.23,0.23


! FR4

MPTEMP
MPTEMP,1,303,368,383,398,423,543

MPDATA,EX,mat_pwf,1,22400,20680,19970,19300,17920,16000
MPDATA,EY,mat_pwf,1,22400,20680,19970,19300,17920,16000
MPDATA,EZ,mat_pwf,1,1600,1200,1100,1000,600,450

! FR4 Poisson's Ratio
MPDATA,NUXY,mat_pwf,1,0.1360,0.1360,0.1360,0.1360,0.1360,0.1360
MPDATA,NUXZ,mat_pwf,1,0.1425,0.1425,0.1425,0.1425,0.1425,0.1425
MPDATA,NUYZ,mat_pwf,1,0.1425,0.1425,0.1425,0.1425,0.1425,0.1425

! FR4 Coefficient of Thermal Expansion
MPDATA,ALPX,mat_pwf,1,20e-6,20e-6,20e-6,20e-6,20e-6,20e-6
MPDATA,ALPY,mat_pwf,1,20e-6,20e-6,20e-6,20e-6,20e-6,20e-6
MPDATA,ALPZ,mat_pwf,1,86.5e-6,86.5e-6,243e-6,400.e-6,400.e-6,400.e-6

! FR4 SHEAR MODULUS
MPDATA,GXY,mat_pwf,1,630,600,550,500,450,441
MPDATA,GXZ,mat_pwf,1,199,189,173,157,142,139.3
MPDATA,GYZ,mat_pwf,1,199,189,173,157,142,139.3
```

File: elements.txt (Element types and numbers)

```
!  element numbers

pl42 = 1                    ! element type of PLANE42
pl82 = 2                    ! element type of PLANE82
sl45 = 3                    ! element type of SOLID45
sl95 = 4                    ! element type of SOLID95

sh91 = 6                    ! element type of SHELL91
sh99 = 7                    ! element type of SHELL99

ET,pl42,PLANE42             ! 2D  4-node structural solid
ET,pl82,PLANE82             ! 2D  8-node structural solid
ET,sl45,SOLID45             ! 3D  8-node structural solid
ET,sl95,SOLID95             ! 3D 20-node structural solid

ET,sh91,SHELL91,,1          ! nonlinear layered structural shell
ET,sh99,SHELL99             ! linear layered structural shell
```

File: BGA_352_eff_sil (Constructs BGA geometry)

```
incc=1e-7

!352 BGA
sub_het = 0.56       ! BGA substrate height
mol_het = 1.17       ! BGA molding height
ball_dia = 0.75       ! BGA ball diameter
ball_sth = 0.45       ! BGA ball standoff height
ball_pit = 1.27       ! BGA ball pitch
sub_len = 35
mol_len = 32.5
mol_cnr = 4
bga_out = 31.75      ! BGA ball matrix outer length
bga_inn = 24.13      ! BGA ball matrix inner length
els_bga =  3          ! BGA size of block mesh element
die_het = 1.0922


pad_rad=sqrt(-(ball_sth/2)**2+(ball_dia/2)**2)             !pad radius

ball_sp=2               !number of lines in quarter circle of ball
sub_sp=2               !number of lines one one edge of molding, PWB, and BGA substrate
sub_versp=2             !number of vertical lines through substrate
mol_versp=2             !number of vertical lines through molding
ball_versp=3            !number of vertical lines through solder ball

!Solder ball geo code
NUMCMP,KP
KSEL,ALL
*GET,ar40,KP,0,NUM,MAX               !   get current max KP number
K,ar40+1, (bga_out+ball_pit)/2, (bga_out+ball_pit)/2,0
K,ar40+2,-(bga_out+ball_pit)/2, (bga_out+ball_pit)/2,0
K,ar40+3,-(bga_out+ball_pit)/2,-(bga_out+ball_pit)/2,0
K,ar40+4, (bga_out+ball_pit)/2,-(bga_out+ball_pit)/2,0
L,ar40+1,ar40+2,nint((bga_out+ball_pit)/els_bga+0.5)
L,ar40+2,ar40+3,nint((bga_out+ball_pit)/els_bga+0.5)
L,ar40+3,ar40+4,nint((bga_out+ball_pit)/els_bga+0.5)
L,ar40+4,ar40+1,nint((bga_out+ball_pit)/els_bga+0.5)
A,ar40+1,ar40+2,ar40+3,ar40+4         !   build area
ar41=_RETURN                          !   area number

K,ar40+5, (bga_inn-ball_pit)/2, (bga_inn-ball_pit)/2,0
K,ar40+6,-(bga_inn-ball_pit)/2, (bga_inn-ball_pit)/2,0
K,ar40+7,-(bga_inn-ball_pit)/2,-(bga_inn-ball_pit)/2,0
K,ar40+8, (bga_inn-ball_pit)/2,-(bga_inn-ball_pit)/2,0
L,ar40+5,ar40+6,nint((bga_inn-ball_pit)/els_bga+0.5)
L,ar40+6,ar40+7,nint((bga_inn-ball_pit)/els_bga+0.5)
L,ar40+7,ar40+8,nint((bga_inn-ball_pit)/els_bga+0.5)
L,ar40+8,ar40+5,nint((bga_inn-ball_pit)/els_bga+0.5)
A,ar40+5,ar40+6,ar40+7,ar40+8         !   build area
ar42=_RETURN                          !   area number

ASBA,ar41,ar42,,DELETE,DELETE
ASEL,S,LOC,X,-sub_len/2,sub_len/2
ASEL,R,LOC,Y,-sub_len/2,sub_len/2
ASEL,R,LOC,Z,0,0
*GET,nae_bgb,AREA,0,NUM,MAX
ESIZE,els_bga                            !   define element division
VOFFST,nae_bgb,ball_sth,0                 !   build volume
num_vol=_RETURN                       !   volume number
                                     ! effective beam model

!*********************************************************************
!Create BT Substrate

NUMCMP,KP
```

```
KSEL,ALL
*GET,ar30,KP,0,NUM,MAX                                  ! get current max KP number
K,ar30+1, sub_len/2, sub_len/2,ball_sth+sub_het          ! build keypoints
K,ar30+2,-sub_len/2, sub_len/2,ball_sth+sub_het
K,ar30+3,-sub_len/2, -sub_len/2,ball_sth+sub_het
K,ar30+4, sub_len/2, -sub_len/2,ball_sth+sub_het

NUMCMP,LINE
LSEL,ALL
*GET,ar35,LINE,0,NUM,MAX                ! get current max LINE number
L,ar30+1,ar30+2,  ! build lines
L,ar30+2,ar30+3,
L,ar30+3,ar30+4,
L,ar30+4,ar30+1,

AL,ar35+1,ar35+2,ar35+3,ar35+4,         ! build area
sub_top=_RETURN

!Create volume
VOFFST,sub_top,-sub_het


!*********************************************************************
!Create molding

NUMCMP,KP
KSEL,ALL
*GET,ar30,KP,0,NUM,MAX                ! get current max KP number
K,ar30+1, mol_len/2-mol_cnr, mol_len/2     ,ball_sth+sub_het+mol_het  ! build keypoints
K,ar30+2,-mol_len/2+mol_cnr, mol_len/2     ,ball_sth+sub_het+mol_het
K,ar30+3,-mol_len/2     , mol_len/2-mol_cnr,ball_sth+sub_het+mol_het
K,ar30+4,-mol_len/2     ,-mol_len/2+mol_cnr,ball_sth+sub_het+mol_het
K,ar30+5,-mol_len/2+mol_cnr,-mol_len/2     ,ball_sth+sub_het+mol_het
K,ar30+6, mol_len/2-mol_cnr,-mol_len/2     ,ball_sth+sub_het+mol_het
K,ar30+7, mol_len/2     ,-mol_len/2+mol_cnr,ball_sth+sub_het+mol_het
K,ar30+8, mol_len/2     , mol_len/2-mol_cnr,ball_sth+sub_het+mol_het

L,ar30+1,ar30+2,  ! build lines
L,ar30+2,ar30+3,
L,ar30+3,ar30+4,
L,ar30+4,ar30+5,
L,ar30+5,ar30+6,
L,ar30+6,ar30+7,
L,ar30+7,ar30+8,
L,ar30+8,ar30+1,

A,ar30+1,ar30+2,ar30+3,ar30+4,ar30+5,ar30+6,ar30+7,ar30+8
mol_top=_RETURN                          ! build area

VOFFST,mol_top,-mol_het,0                      ! build volume
mol_vol=_RETURN                         ! volume number

!*********************************************************************

!CREATE silicon die

NUMCMP,KP
KSEL,ALL
*GET,ar30,KP,0,NUM,MAX                                  ! get current max KP number
K,ar30+1, 6, 6,ball_sth+sub_het+die_het          ! build keypoints
K,ar30+2,-6, 6,ball_sth+sub_het+die_het
K,ar30+3,-6, -6,ball_sth+sub_het+die_het
K,ar30+4, 6, -6,ball_sth+sub_het+die_het

NUMCMP,LINE
LSEL,ALL
*GET,ar35,LINE,0,NUM,MAX                ! get current max LINE number
L,ar30+1,ar30+2,  ! build lines
L,ar30+2,ar30+3,
L,ar30+3,ar30+4,
L,ar30+4,ar30+1,
```

```
AL,ar35+1,ar35+2,ar35+3,ar35+4,         ! build area
die_top=_RETURN

!Create volume
VOFFST,die_top,-die_het
die_vol=_RETURN

VSBV,mol_vol,die_vol,,,KEEP

!Glue the BGA

VSEL,S,LOC,X,-sub_len/2,sub_len/2
VSEL,R,LOC,Y,-sub_len/2,sub_len/2
VSEL,R,LOC,Z,0,ball_sth+sub_het+mol_het
VGLUE,ALL                               ! glue BGA component
NUMCMP,VOLU

VSEL,S,LOC,X,-sub_len/2,sub_len/2
VSEL,R,LOC,Y,-sub_len/2,sub_len/2
VSEL,R,LOC,Z,0,ball_sth+sub_het+mol_het
CM,ncm_bga,VOLU                         ! group BGA component
```

File: BGA_352_mesh_eff_sil1 (Meshes BGA geometry)

```
incc=1e-7

!352 BGA
sub_het = 0.56       ! BGA substrate height
mol_het = 1.17       ! BGA molding height
ball_dia = 0.75       ! BGA ball diameter
ball_sth = 0.45       ! BGA ball standoff height
ball_pit = 1.27       ! BGA ball pitch
sub_len = 35
mol_len = 32.5
mol_cnr = 4
els_bga =  3          ! BGA size of block mesh element
die_het = 1.0922

!Mesh the solder balls
VSEL,S,LOC,X,-sub_len/2,sub_len/2
VSEL,R,LOC,Y,-sub_len/2,sub_len/2
VSEL,R,LOC,Z,0,ball_sth
CM,ncm_bgb,VOLU
VATT,mat_bgb,,sl95                      ! assign volume attributes
MSHKEY,0                                ! use free mesh
MSHAPE,1,3D                             ! use tet-shaped 3D
ESIZE,0.5
VMESH,ncm_bgb                           ! mesh the ball

ALLSEL,ALL
!Mesh the silicon
VSEL,S,,,3
CM,ncm_mol,VOLU
VATT,mat_sil,,sl95                        ! assign volume attributes
MSHKEY,0                                ! use free mesh
MSHAPE,1,3D                             ! use tet-shaped 3D
ESIZE,1
VMESH,ncm_mol

!Mesh the molding
VSEL,S,,,4
CM,ncm_mol,VOLU
VATT,mat_bgm,,sl95                        ! assign volume attributes
MSHKEY,0                                ! use free mesh
MSHAPE,1,3D                             ! use tet-shaped 3D
ESIZE,1.5
VMESH,ncm_mol

!Mesh the substrate
VSEL,S,LOC,X,-sub_len/2,sub_len/2
```

```
VSEL,R,LOC,Y,-sub_len/2,sub_len/2
VSEL,R,LOC,Z,ball_sth,ball_sth+sub_het
CM,ncm_sub,VOLU
VATT,mat_bgm,,sl95                      ! assign volume attributes
MSHKEY,0                               ! use free mesh
MSHAPE,1,3D                            ! use tet-shaped 3D
ESIZE,1.5
VMESH,ncm_sub
```

File: postproc.txt (Creates surface plot and saves warpage results)

```
/POST1

SET,FIRST                       ! read first set

  ALLSEL,ALL
  /VIEW,1  ,0,0,1

  AVPRIN,0,0                    ! average principal key
  PLNSOL,U,Z,0,1                ! contour plot of top surface

  ETABLE,wpg_tbl,U,Z
  ESORT,ETAB,wpg_tbl,0,0
  *GET,tmp_wp1,SORT,,MAX
  *GET,tmp_wp2,SORT,,MIN
  wpg_pwb = tmp_wp1-tmp_wp2       ! calculate warpage

  *CFOPEN,warpage,out,,APPEND             ! save result to file
  *VWRITE,wpg_pwb
  (E20.10)
  *CFCLOS

FINISH
```

REFERENCES

1. Tlusty, George. Manufacturing Processes and Equipment. Prentice Hall, New Jersey, 2000.

2. Tummala, Rao. Fundamentals of Microsystems Packaging. McGraw-Hill, New York, 2001.

3. Lee, Ning-Cheng Lee. Reflow Soldering Processes and Troubleshooting SMT, BGA, CSP, and Flip Chip Technologies. Butterworth-Heinemann, Massachusetts, 2002.

4. http://www.research-intl.com/reflowhandbook/section6.pdf. January, 2005.

5. Yeung, T.S., and M.M.F. Yuen, "Viscoelastic Analysis of IC Package Warpage," Proc. Sensing, Modeling and Simulation of emerging Electronic Packaging, EEP-vol. 17, 101-107, 1996.

6. Tee, T.Y., Sivakumar, K., and L. Haurent, "Warpage Analysis and Viscoelastic Modeling of Block BGA," Proc. Pacific Rim/ASME International Electronic Packaging Technical Conference and Exhibition, 505-511, 2001.

7. Teng, S.Y., Sarihan, V., Thomas, R., and I. Adhihetty, "Impact of Polymerization on Warpage Prediction of Molded Plastic Packages," Proc. Structural Analysis in Microelectronics and Fiber Optics, EEP-vol. 16, 127-131, 1996.

8. Czarnek, R., "Super High Sensitivity Moiré Interferometry with Optical Multiplication," Optics and Lasers in Engineering, 13(2), 87-98, 1990.

9. Qing, X, Wang, G., and F. Dai, "Study of Thermal Deformation of Microelectronics Packaging Product by Interferometric Technique," Acta Mechanica Sinica/Lixue Xuebao, 13(2), 186-192, 1997.

10. Tsai, M., Hsu, C.H.J, and C.T.O. Wang, "Investigation of Thermomechanical Behaviors of Flip Chip BGA Packages During Manufacturing Process and Thermal Cycling," IEEE Transactions on Components and Packaging Technologies, 37(3), 568-576, 2004.

11. Verma, K. and B. Han, "Warpage Measurement of Microelectronic Devices by Far Infrared Fizeau Interferometry," Proc. Thermo-Mechanical Characterization of Evolving Packaging Materials and Structures, EEP-vol. 24, 93-99, 1998.

12. Verma, K., Park, S., and B. Han, "Mechanical Design Parameters for Enhanced Solder Ball Reliability of Flip-Chip PBGA Package Assembly," Proc. Pacific Rim/ASME International Electronic Packaging Technical Conference and Exhibition, 569-575, 2001

13. Yeh, C.P., Banerjee, K., Martin, T., Umeagukwu, C., and R. Fulton, "Experimental and analytical Investigation of Thermally Induced Warpage for Printed Wiring Boards," Proc. 41st Electronic Components & Technology Conference, 382-387, 1991.

14. Yeh, C.P., Ume, C., Fulton, R.E., Wyatt, K.W., and J.W. Stafford., "Correlation of Analytical and Experimental Approaches to Determine Thermally Induced PWB Warpage," IEEE Transactions on Components, Hybrids, and Manufacturing Technology, 16(8), 986-995, 1993.

15. Dang, A.X.H, Ume, I.C., and S. Bhattacharya, "Measurement of Dynamic Warpage During Thermal Cycling of Dielectric Coated SS Substrates for Large Area MCM-D Packaging," Journal of Electronic Packaging, 122, 77-85, 2000.

16. Ding, H., Powell, R.E., Hanna, C.H., and I.C. Ume, "Warpage Measurment Comparison Using Shadow Moiré and Projection Moiré Methods," IEEE Transactions on Components and Packaging Technologies, 25(4), 714-721, 2002.

17. Ding, H., Powell, R.E., and I.C. Ume, "A Projection Moiré System for Measuring Warpage with Case Studies," The International Journal of Microcircuits & Electronic Packaging, 25(1), 15-26, 2003.

18. Ding, H., "Prediction and Validation of Thermomechanical Reliability in Electronic Packaging," PhD Dissertation, Georgia Institute of Technology, 2003.

19. Stiteler, M. R., Ume, I.C., and B. Leutz, "In-Process Board Warpage Measurement in a Lab Scale Wave Soldering Oven," IEEE Transactions on Components, Packaging, and Manufacturing Technology, 19(4), 562-569, 1996.

20. Stiteler, M.R. and I.C. Ume, "System for Real-Time Measurement of Thermally Induced PWB/PWA Warpage," ASME Journal of Electronic Packaging, 119, 1-7, 1997.

21. Mittal, S., Masada, G., and T. Bergman, "Mechanical Response of PCB Assemblies During Infrared Reflow Soldering," IEEE Transactions on Components, Packaging, and Manufacturing Technology, 19(1), 127-133, 1996.

22. Polsky, Y., Ume, C, and W. Sutherlin, "Application of Thermoelastic Lamination Theory to Predict Warpage of a Symmetric and Simply Supported Printed Wiring Board During Temperature Cycling," Proc. 48th Electronic Components & Technology Conference, 345-352, 1998.

23. Polsky, Y. and I.C. Ume, "Thermoelastic Modeling of a PWB with Simulated Circuit Traces Subjected to Infrared Reflow Soldering with Experimental Validation," Journal of Electronic Packaging, 121, 1-8, 1999.

24. Polsky, Y., Sutherlin, W. and I.C. Ume, "A Comparison of PWB Warpage Due to Simulated Infrared and Wave Soldering Processes," IEEE Transactions on Electronics Packaging Manufacturing, 23(3), 191-199, 2000.

25. Wu, J.C.L., Shiue, H., Wu, S., Hung, M., and J.J. Lee, "Study of Rapid Cure BGA Mold Compound on Warpage with Shadow Moiré," Proc. Electronic Components and Technology Conference, 708-713, 1999.

26. Djurovic, B., Puzzo, C.A. and J.K. Spelt, "Analysis of Thermal Warpage in a PCB with an Array of PTH Connectors," IEEE Transactions on Components and Packaging Technology, 22(3), 414-420, 1999.

27. Muncy, J., Ding, H., Baldwin, D., Ume, I.C. and M. Richmond, "Thermally Induced Out of Plane Deformation Analysis for a Flip Chip on Flex 35MM TBGA," Proc. Surface Mount Association Technology International Conference, 284-288, 2003.

28. Ding, H., Ume, I. C., Zhang, J., and D. F. Baldwin, "Integrated Hardware and Software for Improved Flatness Measurement with ATC4.1 Flip-Chip Assembly Case Study," IEEE Transactions on Instrumentation and Measurement, 54(5), 1898-1904, 2005.

29. Zewi, I.G., Daniel, I.M., and J.T. Gotro, "Residual Stresses and Warpage in Woven-Glass/Epoxy Laminates," Experimental Mechanics, 27(1), 44-50, 1987.

30. Karalekas, D., and I.M. Daniel, "The Influence of Lamination Parameters on Warpage of Woven-Glass/Epoxy Laminates," Proc. Society of Plastics Engineers 45th Annual Technical Conference & Exhibit, 339-342, 1987.

31. Daniel, I.M., Wang, T.M., and J.T. Gotro, "Thermomechanical Behavior of Multilayer Structures in Microelectronics," ASME Journal of Electronic Packaging, 112, 11-15, 1990.

32. Wang, T.-M., Daniel, I.M. and J.T. Gotro, "Thermoviscoeleastic Analysis of Residual Stresses and Warpage in Composite Laminates," Journal of Composite Materials, 26(6), 883-899, 1992.

33. He, X., and S. Liu, "Real-Time Warpage Measurement of a Plastic BGA by Projected Grating Method," Proc. International Symposium on Microelectronics, 537-542, 1998.

34. Petriccione, G.J. and I.C. Ume, "Warpage Studies of HDI Test Vehicles During Various Thermal Profiling," IEEE Transactions on Advanced Packaging, 22(4), 624-637, 1999.

35. Dang, A.X.H., Ume, I.C., and S.K. Bhattacharya, "A Study on Warpage of Flexible SS Substrates for Large Area MCM-D Packaging," ASME Journal of Electronic Packaging, 122, 86-91, 2000.

36. Dang, A.X.H., Ume, I.C., and S.K. Bhattacharya, "Process Induced warpage in Multitiled Alumina Substrates for Large Area MCM-D Processing," IEEE Transactions on Advanced Packaging, 23(3), 436-446, 2000.

37. Bhattacharya, S.K., Ume, I.C., and A.X.H. Dang, "Warpage Measurement of Large Area Multitiled Silicon Substrates at Various Processing Conditions," IEEE Transactions on Components and Packaging Technology, 23(3), 497-504, 2000.

38. Bhattacharya, S.K., "Warpage of Conductive Gallium Alloy Via-Filled Stainless Steel Substrates For Large Area Microelectronic Packaging," The International Journal of Microcircuits and Electronic Packaging, 23(3), 309-319, 2000.

39. Banerji, S., Raj, P.M., Liu, F., Shinotani, K., Bhattacharya, S. and R. Tummala, "The Role of Stiff Base Substrates in Warpage Reduction for Future High-Density-Wiring Requirements," Proc. 8th International Symposium on Advanced Packaging Materials, 221-225, 2002.

40. Bansal, S., Raj, P.M., Shinotani, K., Bhattacharya, S.K., Tummala, R. and M.J. Lance, "In-situ Stress and Warpage Measurements to Investigate Reliability of Flip-Chip on Board Assembly without Underfill," Proc. 53rd Electronic Components and Technology Conference, 148-155, 2003.

41. Bansal, S., Raj, P.M., Shinotani, K., Bhattacharya, S.K., Tummala, R. and M.J. Lance, "Reliability Assessment of High Density Multi-Layer Board Assembly Using Shadow Moiré and Luminescence Spectroscopy," Proc. Electronic Packaging Technology Conference, 126-132, 2002.

42. Han, B., Guo, Y. and H. Choi, "Out-of-Plane Displacement Measurement of Printed Circuit Board by Shadow Moiré with Variable Sensitivity," Proc. of the 1993 ASME International Electronics Packaging Conference, 179-185, 1993.

43. Zhang, J., Ding, H., Baldwin, D. and I.C. Ume, "In-Process Stress Characterization of Flip Chip Assembly on Warped Organic Substrate," Proc. 53rd Electronic Components and Technology Conference, 2003.

44. Ham, S., and S. Lee, "Measurement of Thermo-mechanical Deformation of Wafer-Level CSP Assembly Under Thermal Cycling Condition," Proc. International Symposium on Electronic Materials and Packaging, 323-327, 2001.

45. Wang, Y. and P. Hassell, "Measurement of Thermally Induced Warpage of BGA Packages/Substrates Using Phase-Stepping Shadow Moire," Proc. IEEE/CPMT Electronic Packaging Technology Conference, 283-289, 1997.

46. Wang, Y. and P. Hassell, "On-Line Measurement of Thermally Induced Warpage of BGAs with High Sensitivity shadow Moiré," The International Journal of Microcircuits and Electronic Packaging, 21(2), 191-196, 1998.

47. Shook, R.L., Gilbert, J.J., Thomas, E., Vaccaro, B.T., Dairo, A., Horvath, C., Libricz, G.J., Crouthamel, D.L., and D.L. Gerlach, "Impact of Ingressed Moisture and High Temperature Warpage Behavior on the Robust Assembly Capability for Large Body PBGAs," Proc. Electronic Components and Technology Conference, 1823-1828, 2003.

48. Wu, S., Lu, H., Yang, T., and C. Yeh, "Process Induced Warpage and Residual Stress in Populated Ball Grid Array Substrate Panel," Proc. International Symposium on Advanced Packaging Materials, 151-152, 1998.

49. Liang, D., "Warpage Study of Glob Top Cavity-up EPBGA Packages," Proc. Electronic Components and Technology Conference, 694-701, 1996.

50. Wang, W., and Y. Liu, "Measurement of Warpage of Electronic Packagings after Machining by Phase-shifting Shadow Moire Method," Proc. Third International Conference on Experimental Mechanics, 20-24, 2002.

51. Fu, C. and C. Ume, "Characterizing the Temperature Dependence of Electronic Packaging-Material Properties," Journal of Minerals, Materials and Metals, 47(6), 31-35, 1995.

52. Ume, I.C., Martin, T. and J.T. Gatro, "Finite Element Analysis of PWB Warpage Due to the Solder Masking Process," IEEE Transactions on Components, Packaging, and Manufacturing Technology, 20(3), 295-306, 1997.

53. Ume, I.C., and T. Martin, "Finite Element Analysis of PWB Warpage Due to Cured Solder Mask – Sensitivity Analysis," IEEE Transactions on Components, Packaging, and Manufacturing Technology, 20(3), 307-316, 1997.

54. Dunne, R.C. and S.K. Sitaraman, "An Integrated Process Modeling Methodology and Module for Sequential Multi-layered Substrate Fabrication using a Coupled Cure-Thermal-Stress Analysis Approach," Proc. Electronic Components and Technology Conference, 1311-1319, 2000.

55. Ding, H, Powell, R.E., Hanna, C.R., and I.C. Ume, "A Finite Element Modeling Methodology for Thermomechanical Analysis of Printed Wiring Board Assemblies," Proc. Electronic Components and Technology Conference, 410-414, 2003.

56. Ding, H, Ume, I. C., Powell, R. E. and C. R. Hanna, "Parametric Study of Warpage in Printed Wiring Board Assemblies," IEEE Transactions on Components and Packaging Technologies, 28(3), 517-524, 2005.

57. Yao, Q., and J. Qu, "Effects of PWB Size on the Warpage of Flip Chip Assemblies," Proc. of InterPACK '99, ASME EEP, 121(3), 196-201.

58. Yang, S., Jiang, S., and W. Lu, "Ribbed Package Geometry for Reducing Thermal Warpage and Wire Sweep During PBGA Encapsulation," IEEE Transactions on Components and Packaging Technologies, 23(4), 700-706, 2000.

59. Moore, T.D., and J.L. Jarvis, "The Effects of In-Plane Orthotropic Properties in a Multi-Chip Ball Grid Array Assembly," Microelectronics Reliability, 42, 943-949, 2002.

60. Li, Y., "Accurate Predictions of Flip Chip BGA Warpage," Proc. Electronic Components and Technology Conference, 549-553, 2003.

61. Chong, D.Y.R., Wang, C.K., Fong, K.C., and P. Lall, "Finite Element Parametric Analysis on Fine-Pitch BGA (FBGA) Packages," Proc. Pacific Rim/ASME International Electronic Packaging Technical Conference and Exhibition, 933-939, 2003

62. Xie, D., Arra, M., Yi, S., and D. Rooncy, "Solder Joint Behavior of Area Array Packages in Board Level Drop for Handheld Devices," Proc. Electronic Components and Technology Conference, 130-135, 2003.

63. Amagai, M., "Characterization of Chip Scale Packaging Materials," Microelectronics Reliability, 39, 1365-1377, 1999.

64. Zhang, X., and T.Y. Tee, "Advanced Warpage Prediction Methodology for Matrix Stacked Die BGA During Assembly Processes," Proc. Electronic Components and Technology Conference, 593-600, 2004.

65. Zwemer, D., Bajaj, M., Peak, R., Thurman, T., Brady, K., McCarron, S., Spradling, A., Klein, L., Dickerson, M., Liutkus, G., and J. Messina, (2004). PWB Warpage Analysis and Verification Using an AP210 Standards-based Engineering Framework and Shadow Moiré . EuroSimE 2004, Brussels, Belgium.

66. Bajaj, M., Peak, R. S., Zwemer, D. A., Dickerson, M., Thurman, T., Brady, K., and J. Messina (2005) Next Generation Simulation-based Design Technologies for Electronics Product Realization. 7th NASA-ESA Workshop on Product Data Exchange (PDE): The Workshop for Open Product & System Lifecycle Management (PLM/SLiM), Atlanta.

67. Peak, R. S. (2005) A Multi-Representation Architecture for STEP AP210-based PCB/PCA Stackup Design and Warpage Analysis. InterCAX LLC Phase 1 Project, NIST SBIR FY05 Program

68. Zeng, S., Peak, R., Matsuki, R., Xiao, A., Wilson, M., Fulton, R. E. "An Information-Driven FEA Model Generation Approach for Chip Package Applications", ASME, 23rd Computers and Information in Engineering Conference, September 2-6, Chicago, Illinois. 2003.

69. Zeng, S., "Knowledge-based FEA Modeling for Highly Coupled Variable Topology Multi-body Problems," PhD Dissertation, Georgia Institute of Technology, 2004.

70. Dahle, B. and R. Lasky, "Optimizing Reflow: Successful Reflow Soldering is Key to Productivity and Profitability," SMT, January 2004, 40-42.

71. Incropera, F. P. and D. P. DeWitt. Fundamentals of Heat and Mass Transfer, Fourth Edition. John Wiley & Sons. (1996)

72. http://www.matweb.com. January, 2005.

73. Wu, C.F. Jeff, and Michael Hamada. Experiments: Planning, Analysis, and Parameter Design Optimization. John Wiley & Sons. (2000)

74. Gonzalez, R. C., and R. Woods. Digital Image Processing. Prentice Hall, New Jersey, 2001.

75. Canny, J. "A Computational Approach to Edge Detection," IEEE Transactions on Pattern Analysis and Machine Intelligence, 8(6), 1986.

76. Steger, C., "Similarity Measures for Occlusion, Clutter, and Illumination Invariant Object Recognition," Proc. 23rd DAGM-Symposium on Pattern Recognition, 148-154, 2001.

77. Kass, M, Witkin, A., and D. Terzopoulos., "Snakes: Active Contour Models," International Journal of Computer Vision, 321-331, 1988.

78. Williams, D., and M. Shah, "A Fast Algorithm for Active Contours and Curvature Estimation," CVGIP: Image Understanding, 55(1), 14-26, 1992.

79. Muncy, J., "Predictive Failure Model for Flip Chip on Board Component Level Assemblies," PhD Dissertation, Georgia Institute of Technology, 2004.

VITA

Reinhard Powell was born in Kingston, Jamaica to Pamella Powell and Granville Powell. He attended Hillel Academy High School in Kingston, Jamaica and graduated in 1995. He graduated with a Bachelor of Science in Mechanical Engineering from Georgia Tech in 2000 and a Master of Science in Mechanical Engineering from Georgia Tech in 2003. He received the Woodruff School Pi Tau Sigma Outstanding Senior award in 2000 and the Georgia Tech Manufacturing Research Center Manufacturing Education Program Fellowship in 2001. During the summer of 2001, he worked as a mechanical engineering intern at Dell Computer Corporation. In 2004, he was chosen to be a Sam Nunn International Security Fellow and studied national and international security policy issues. In July 2005, he married Tam'ra Osborne, a fellow Georgia Tech alum. His personal interests are motorsports, most sports and community service.